HTS Materials and Devices for Digital Applications

John Talvacchio
Northrop Grumman Corporation, Baltimore, MD

- **Motivation for HTS Josephson-based electronics**
- **Junction status**
  - **Junction configurations**
  - **Progress in meeting desired junction parameters**
  - **What we think we understand**
- **Multilayer process development**
- **Some example HTS circuits**
- **Specific applications of interest to Northrop Grumman**
  - **A/D converters**
  - **D/A converters**
- **Issues & Summary**
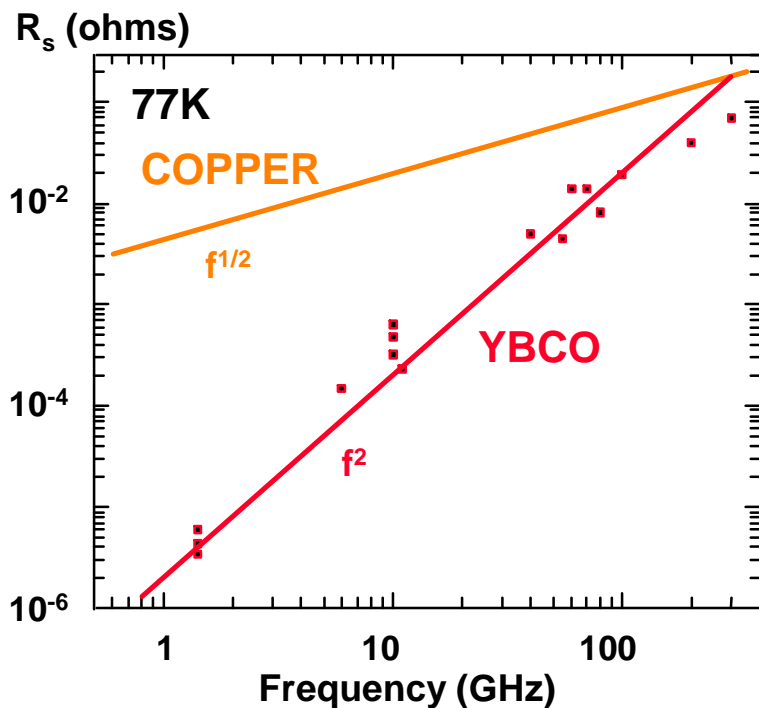
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HTS Materials and Devices
for Digital Applications: Bibliography

These papers are written by Northrop Grumman authors whose material is mainly used in this presentation. Other relevant papers can be found in the same sources, particularly in the proceedings of the 1998 Applied Superconductivity Conference published in Vol. 9 No. 2 of the *IEEE Trans. on Applied Superconductivity* (1999).
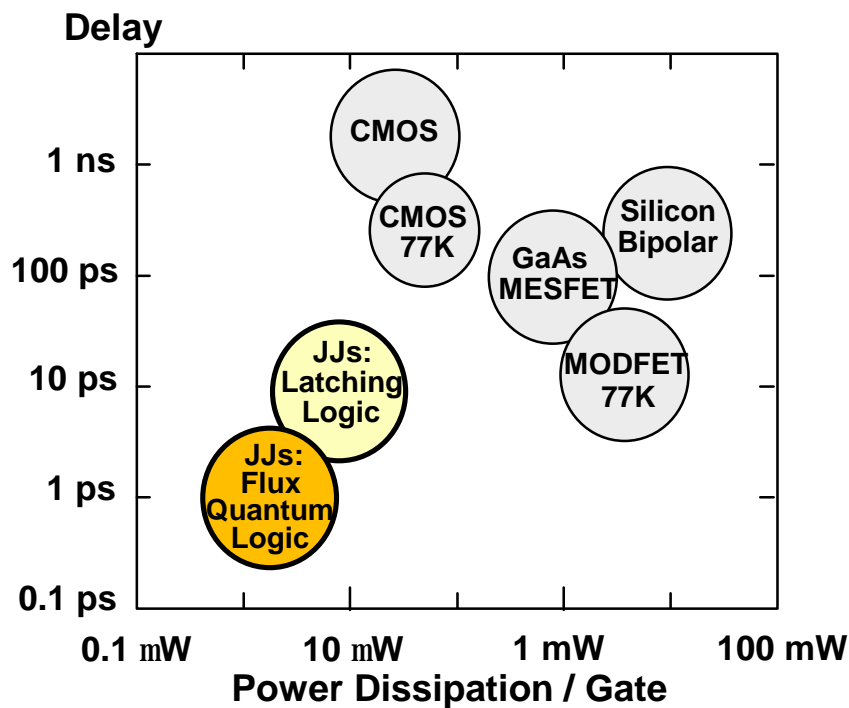
- B. D. Hunt, M. G. Forrester, and J. Talvacchio, "HTS Josephson Junction Development," in *Encyclopedia of Electrical and Electronics Engineering*, edited by J. G. Webster (John Wiley & Sons, New York, 1999).

- J. X. Przybysz, S. B. Kaplan, D. L. Miller, and S. V. Rylov, "Superconducting Analog to Digital Converters," in *Encyclopedia of Electrical and Electronics Engineering*, edited by J. G. Webster (John Wiley & Sons, New York, 1999).

- B. D. Hunt, M. G. Forrester, J. Talvacchio, and R. M. Young, "High-Resistance HTS Edge Junctions for Digital Circuits," IEEE Trans. on Applied Superconductivity 9(2), 3362 (1999).

- J. Talvacchio, M. G. Forrester, B. D. Hunt, J. D. McCambridge, R. M. Young, and X. F. Zhang, and D. J. Miller, "Materials Basis for a Six-Level Epitaxial HTS Digital Circuit Process," IEEE Trans. on Applied Superconductivity 7(2), 2051 (1997).

- M. G. Forrester, B. D. Hunt, D. L. Miller, J. Talvacchio, and R. M. Young, "Analog Demonstration of an HTS Sigma-Delta Modulator with 27 GHz Sampliing," Supercond. Sci. Technol. 12(11) 698-700 (1999).

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Orders of Magnitude Performance Advantage From Superconductivity and Cryogenics

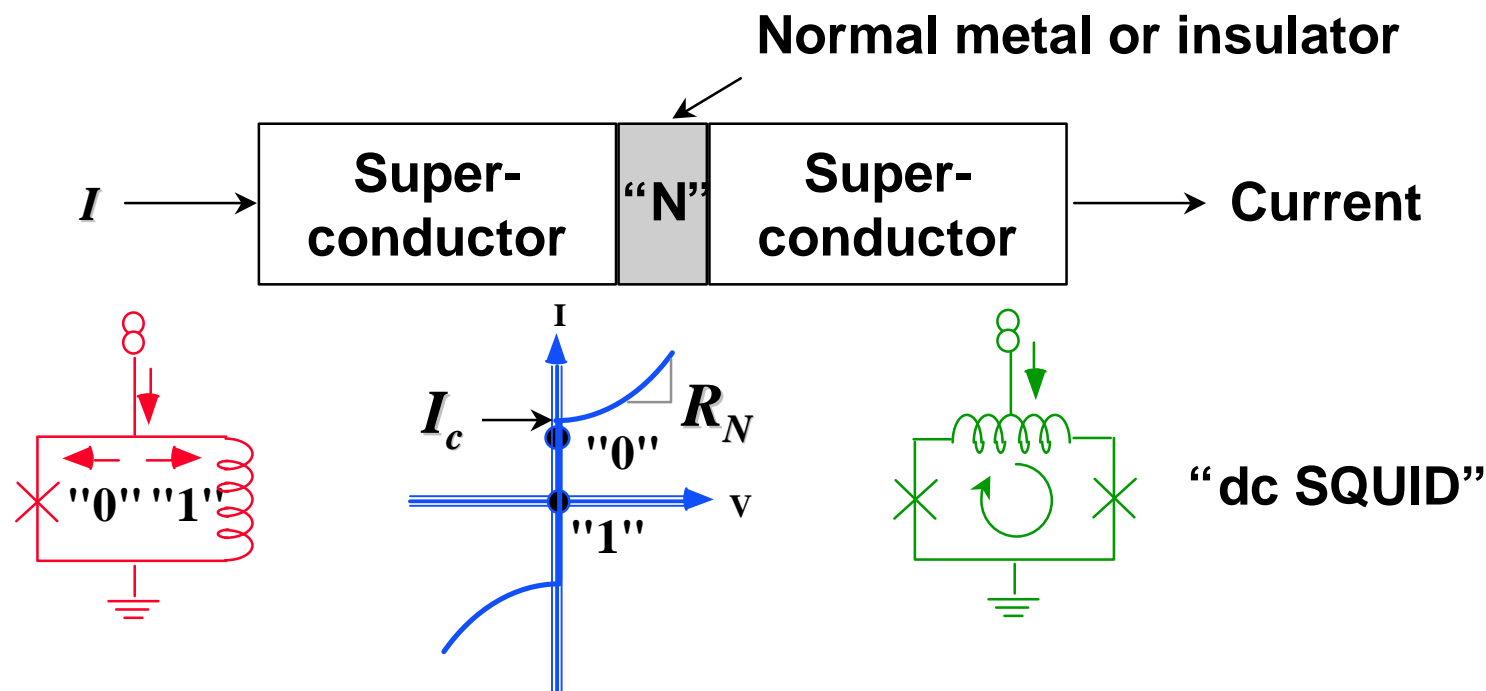**1. Low Surface Resistance: Improved Performance of Microwave Devices**

2. Reduced Power Dissipation and Delay: High-Speed Logic

R$_s$ (ohms)

77K

COPPER

$f^{1/2}$

YBCO

f^2

10^{-2}

10^{-4}

10^{-6}

1   10   100

Frequency (GHz)

Delay

CMOS

CMOS 77K

Silicon Bipolar

GaAs MESFET

JJs: Latching Logic

MODFET 77K

JJs: Flux Quantum Logic

1 ns

100 ps

10 ps

1 ps

0.1 ps

0.1 mW   10 mW   1 mW   100 mW

Power Dissipation / Gate

3. Unique Quantum Accuracy: Voltage Standard, DAC, ADC

4. Low Noise from Cryogenic Operation

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Josephson Junctions are the Building Blocks of Superconducting Digital Circuits

Normal metal or insulator

| I → | Super-conductor | "N" | Super-conductor | → Current |

"0" "1"

I_c → "0" R_N V "1"

"dc SQUID"

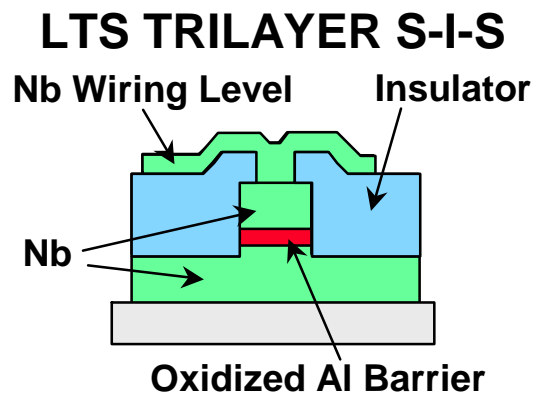**Picosecond transition between states**
- *~100 GHz clock speed attainable*

Digital "1" & "0" both zero voltage
- *low power dissipation (μW/gate)*

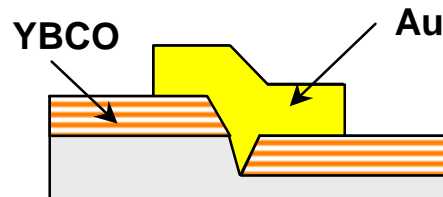$$I = I_c \sin(f_L - f_R)$$

$$V = \frac{\hbar}{2e} \frac{df}{dt}$$

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HTS vs. LTS Junction Configurations

LTS TRILAYER S-I-S

Nb Wiring Level   Insulator

Nb

Oxidized Al Barrier

LTS Junctions:

- **< 150ºC processing**
- **randomly-oriented, polycrystalline films**
- **single-component films**
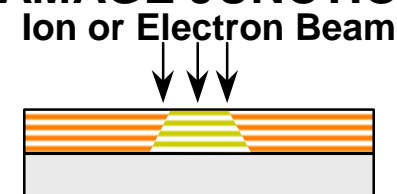- **silicon substrates**
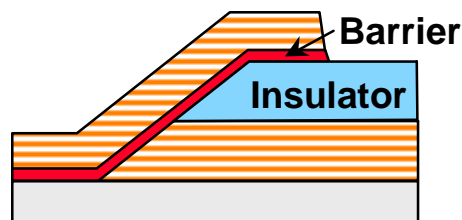- **level of integration = 10,000s**

STEP-EDGE S-N-S

YBCO   Au

STEP-EDGE GRAIN BOUNDARY

Grain boundaries formed at step
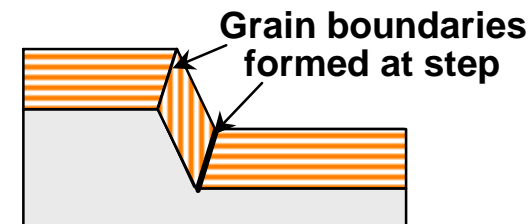
HTS Junctions:

- **750ºC processing**
- **epitaxial, oriented films**
- **single-crystal oxide substrates**
- **level of integration = 10s**

DAMAGE JUNCTIONS

Ion or Electron Beam

EDGE S-N-S

Barrier

Insulator

TRILAYER S-N-S

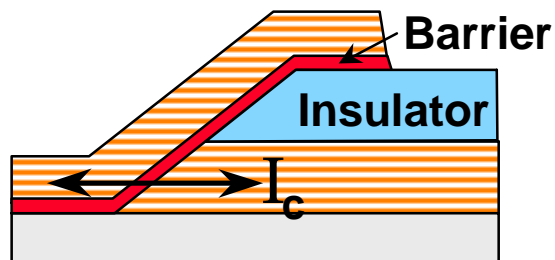Wiring level   Insulator

a-axis YBCO film   Barrier
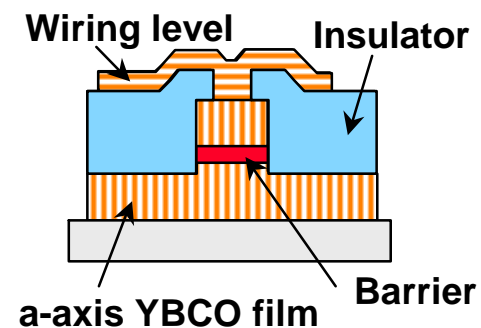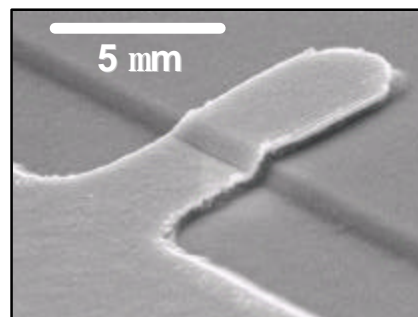
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Selection of an HTS Junction Configuration: Edge S-N-S Junctions
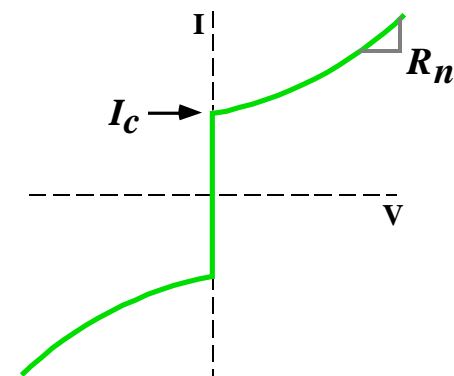
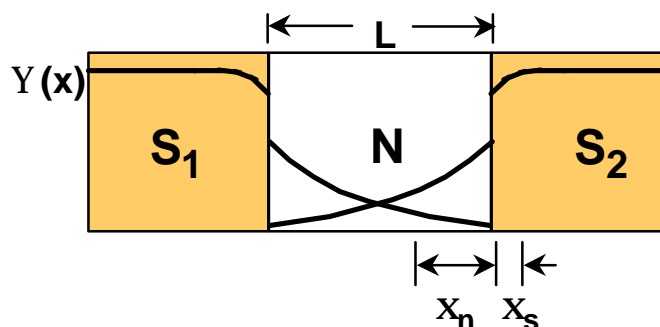**Schematic**   **SEM Micrograph**   **I-V Curve**

Major Advantages of Edge SNS Junctions

- Contact to long-x_n and long-x_s directions of c-axis films

- 50 - 100 Å bridge lengths, L
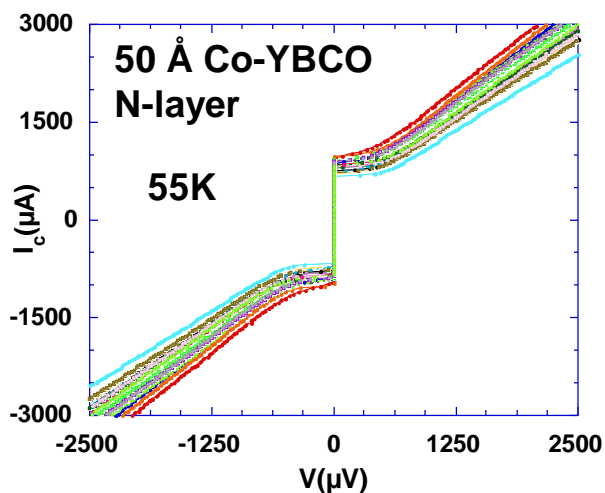 (LTS junctions use ~ 8 Å thick tunnel barriers)

- Small device areas ➨ high R_n

$$I_c \propto e^{-L/x_n}$$

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Progress in Meeting
Required HTS Junction Parameters

- **Single Flux Quantum designs require** $LI_c \gg \Phi_o = 2$ **pH-mA**

- **Thermal noise constraints require** $I_c \gg 0.5$ **mA** ✓
  - ➤ **SQUIDs must have low** $L \gg 4$ **pH** ✓
  - ➤ **Must use an integrated HTS ground plane** ✓
  - ➤ **Junctions must face in several directions** ✓

- **High** R_n **(~ 2 Ω) for digital output signals: max V =** $I_c R_n$ ✓

- **Low** R_n **(~ 0.01 Ω) for ac voltage standards** ✓

- **Circuit margins limit** I_c **variation**   **(we are working on it)**

**50 Å Co-YBCO
N-layer**

55K

I_c (μA) vs V(μV)

Average Junction Parameters:

- $I_c = 834$ μA, $\sigma_{Ic} = 10\%$
- $I_c R_n = 797$ μV, $\sigma_{IcRn} = 6\%$
- $R_n = 0.96$ Ω, $\sigma_{Rn} = 5\%$

Inductance (pH/sq)

**mstrip inductance
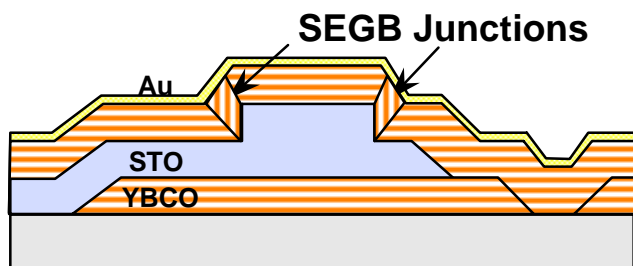goal of 1 pH/sq (65K)
achieved**

Temperature (K)
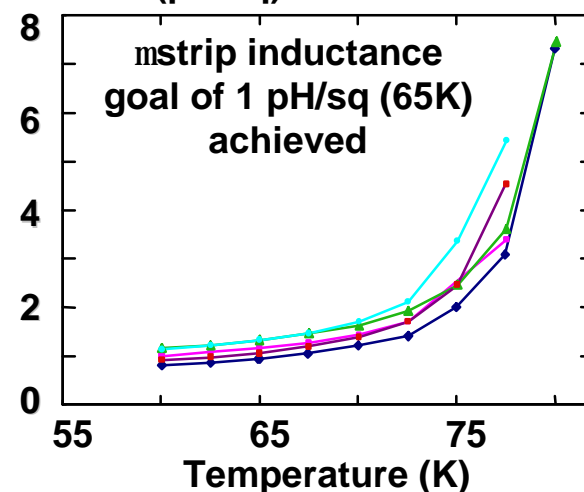
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Integrated HTS Groundplane Required for Low Inductance

- **Achieved for two junction technologies**

SEGB Circuit Cross Section

SNS Circuit Cross Section

SEGB Junctions

SNS Junction

Au

Au

STO

STO

YBCO

YBCO

- **Simpler process but I_c spread ~ 30%**
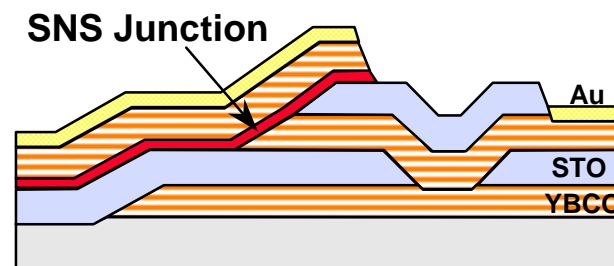
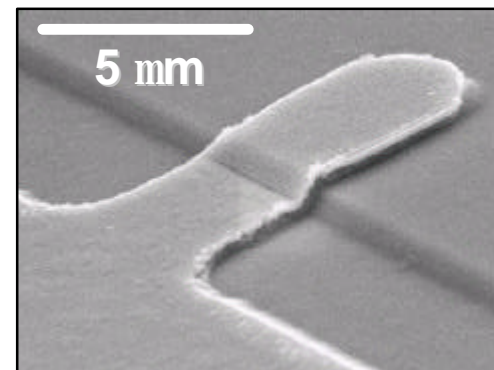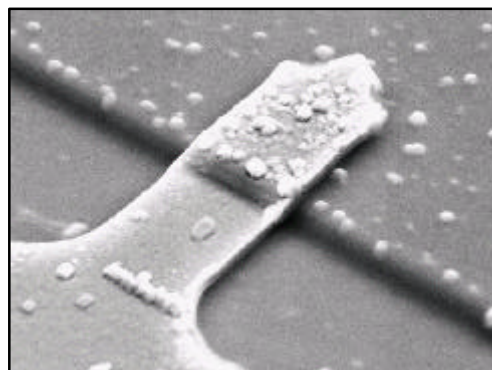- **More complex process but I_c spread ~ 12%**
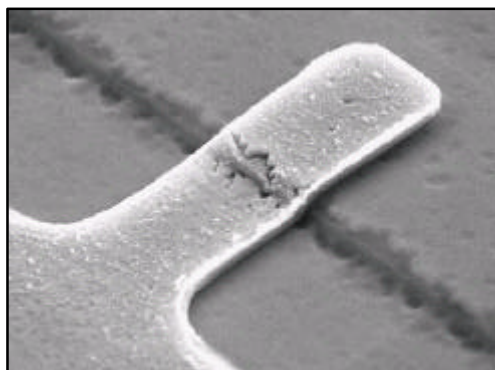
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Disadvantage of a Point Compound: CuO "Boulders"

XTEM of a boulder grown in the top YBCO layer
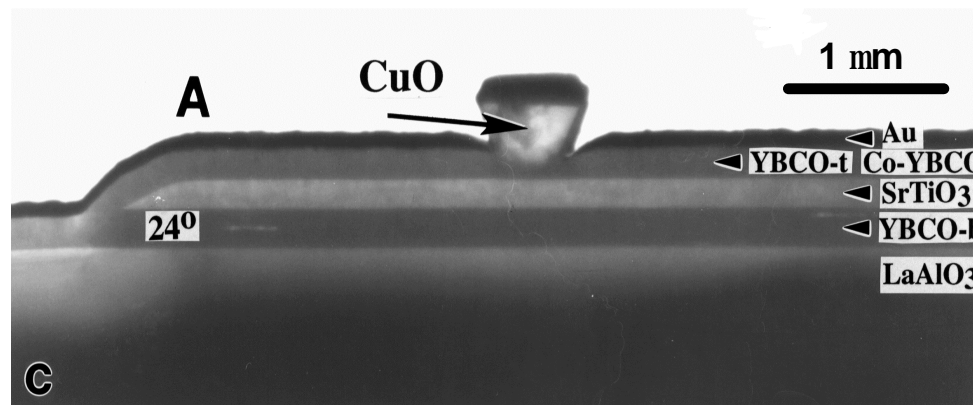
Step Coverage
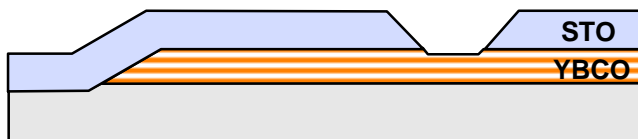- **Top YBCO deposited under three different conditions**

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Major Processing Steps for Edge Junctions on a Groundplane

1. Groundplane

YBCO

2. Groundplane Insulator

STO
YBCO

3. Base Electrode / Insulator Bilayer

STO
YBCO
STO
YBCO
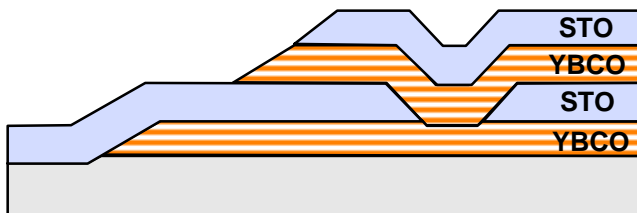
4. N-Layer, Top Electrode, Contact

Au
Normal Metal
YBCO
STO
YBCO
STO
YBCO
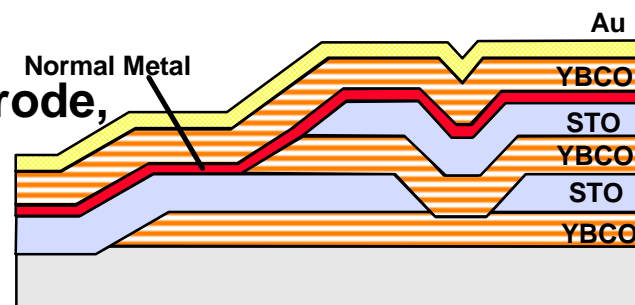
5. Via Holes, Ex-situ Contacts

Au
STO
YBCO
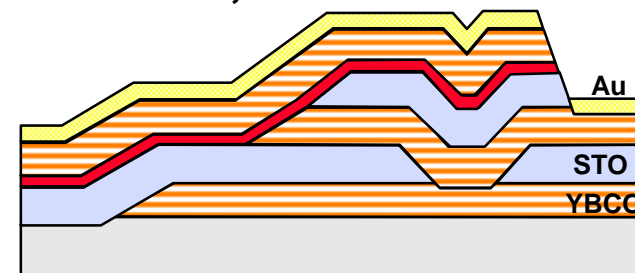
6. Counterelectrode Patterning

Au
STO
YBCO

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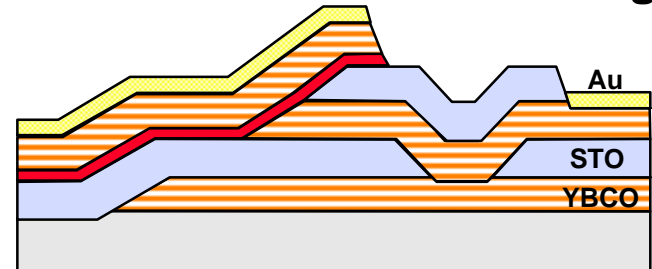
Alternative Configuration Tested: Groundplanes on Top

YBCO Groundplane

STO

YBCO   YBCO

substrate

Normal metal
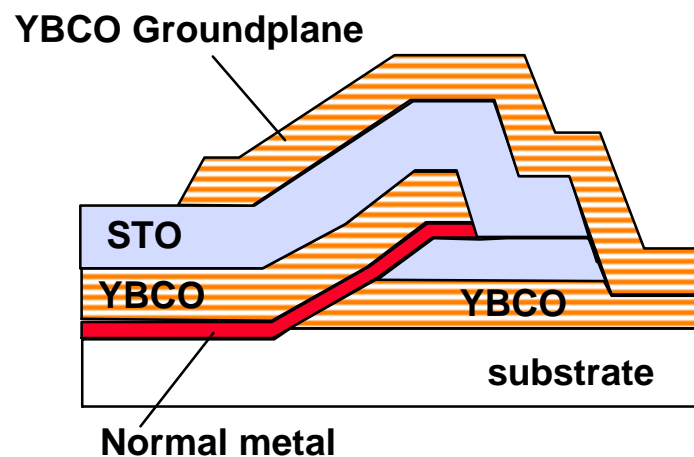
- **<u>Potential Advantages:</u>**
- **Simplified, more forgiving process**
- **Tighter junction spreads**
- **Passivation**

65 K

1000

500

0

Ic(μA)

-500

-1000

-400   -200   0   200   400

V(μV)
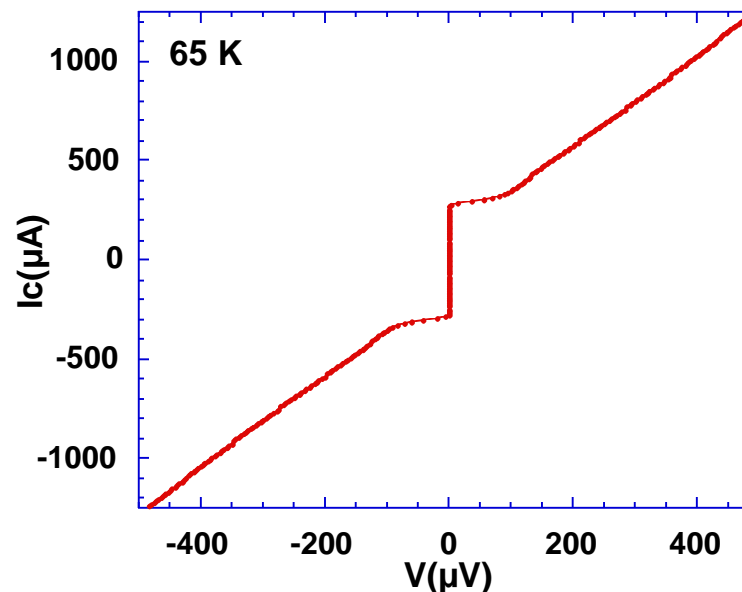
- **High quality I-V characteristics, - same as control chip without groundplane**
- **Junctions survived high temp. processing**
- **Groundplane effectiveness under study**

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Control of SNS Junction Resistance

- **High R_n for HTS digital circuits, ~ 1 Ω**

- **Low R_n for D/A converters, ~ 0.01 Ω**

- **In either case, good fit to proximity effect model**

Resistance depends on effective area:

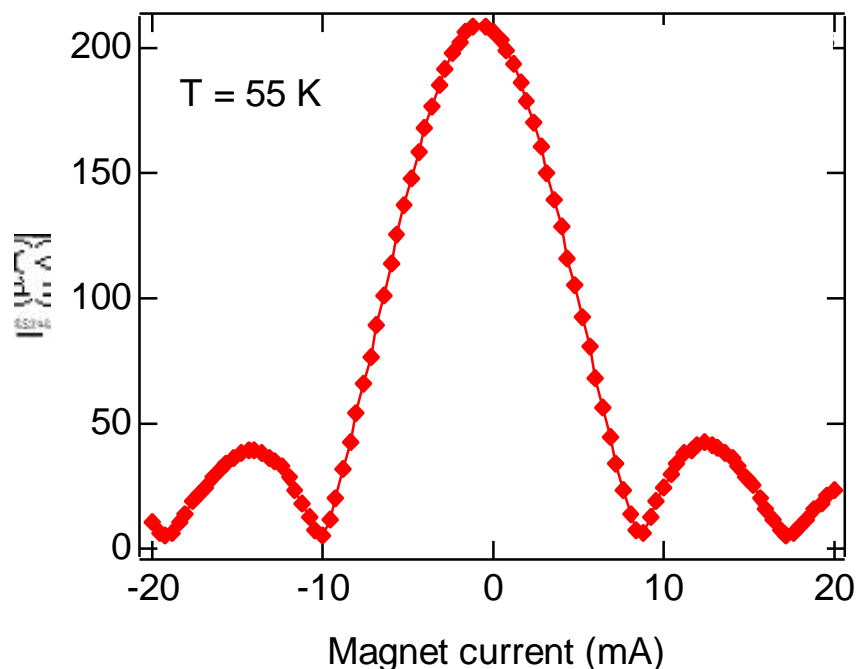- **Conduction is uniform by $I_c(B)$ and I_c spreads**

To increase R_n:

- **N-layer composition: Higher Co-content**
- **Thicker N-layer**
- **Shallower edge angle**
- **Base electrode composition:**
  La-doping $\Rightarrow$ higher R_n than 1:2:3 YBCO
  sputtered 1:2:3 $\Rightarrow$ higher R_n than PLD 1:2:3
- **Cleaning of base electrode edge:**
  Br etch $\Rightarrow$ 3-5x lower R_n than ion milling
- **Deposition parameters of N-layer and top electrode**
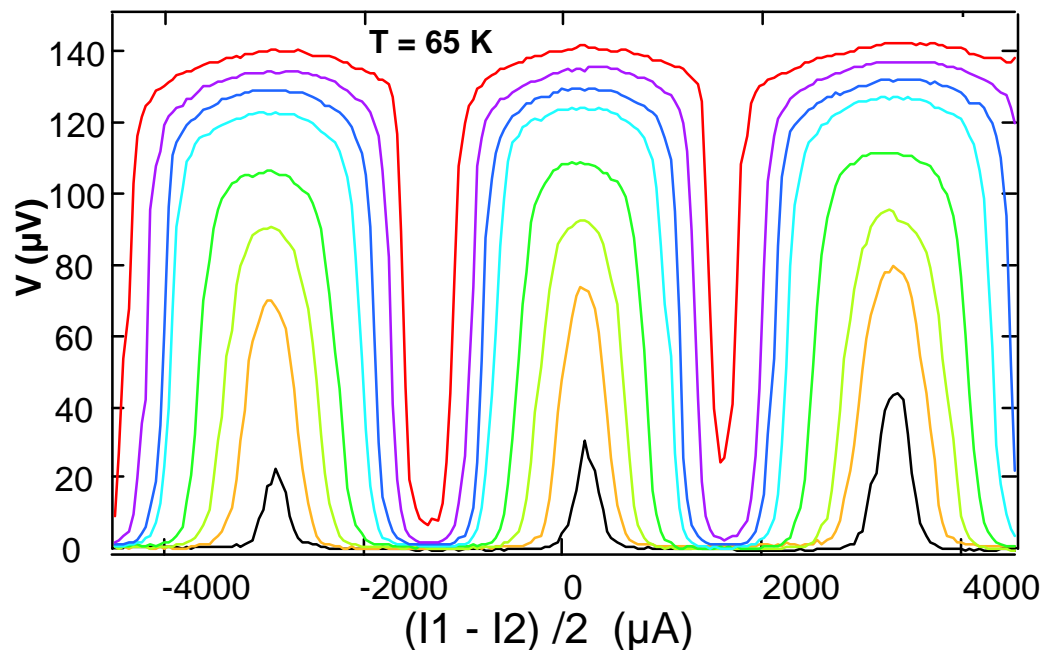
These factors apply even without N-layer

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Expected Behavior Observed for Modulation in Magnetic Fields

Single-Junction $I_c(B)$

T = 55 K

Magnet current (mA)

SQUID Voltage Modulation

T = 65 K

V (µV)

(I1 - I2) /2 (µA)

- **Nearly ideal $I_c(B)$ modulation suggests uniform current density** *on the scale of the junction area – may be inhomogeneous on a much finer scale*
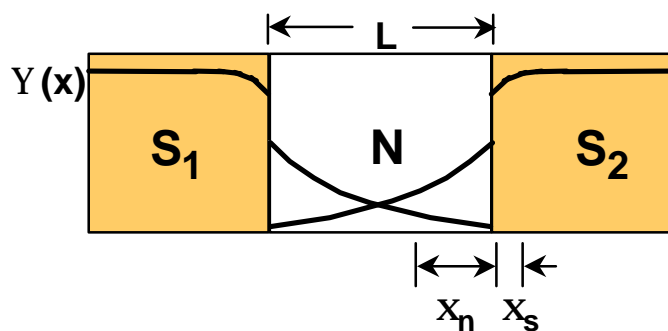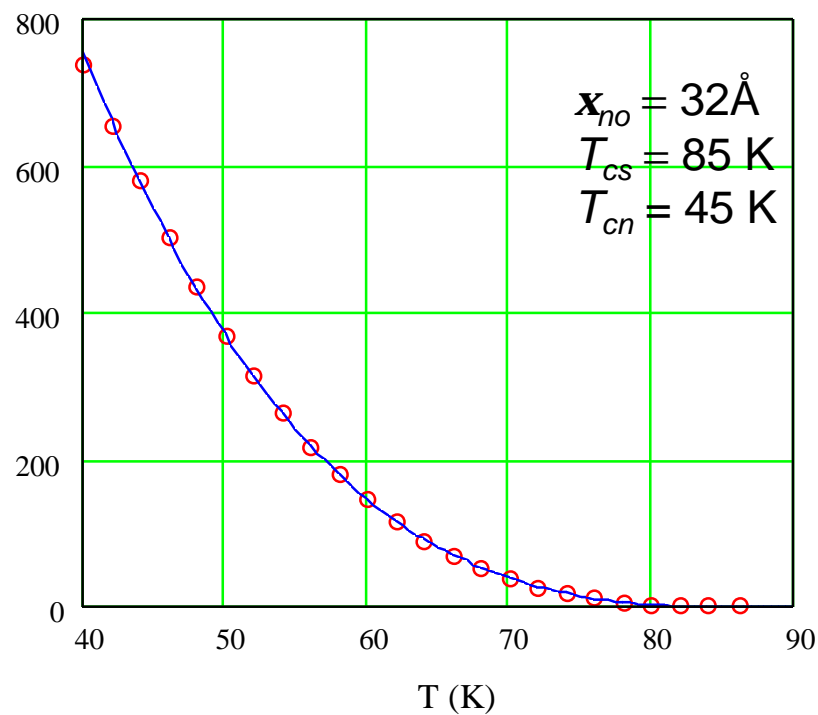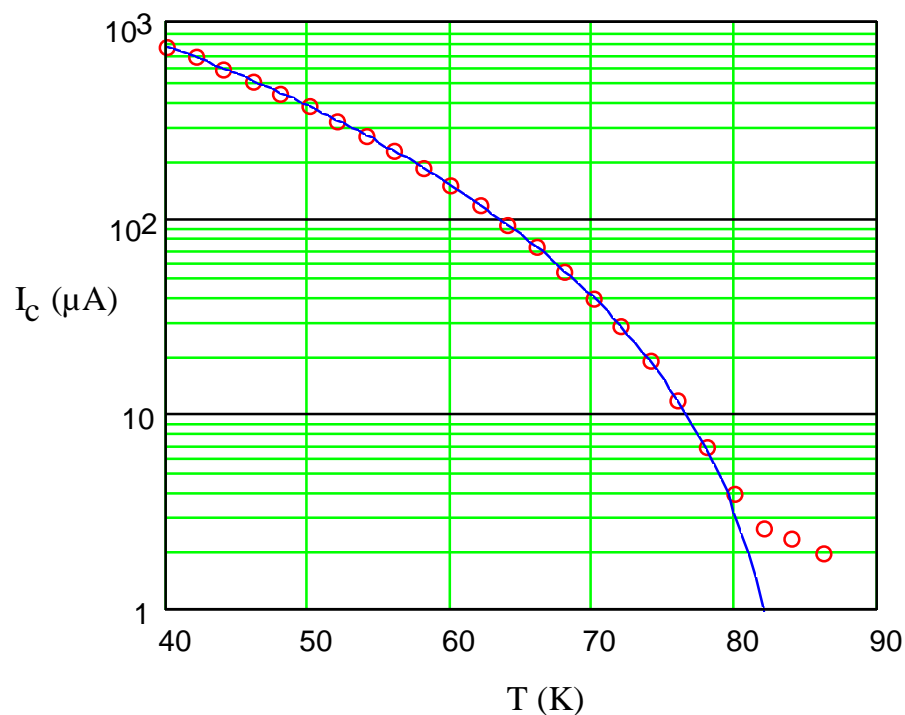
- **Voltage modulation up to 135 µV at 65 K**

- **Microstrip inductance ~ 1 pH / sq. at 65K** *– suitable for SFQ circuits*

- *Total* **SQUID inductance as low as 4.5 pH**

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$I_c(T)$ Fit to Proximity Effect Model Demonstrates SNS Behavior

$x_{no} = 32\text{Å}$
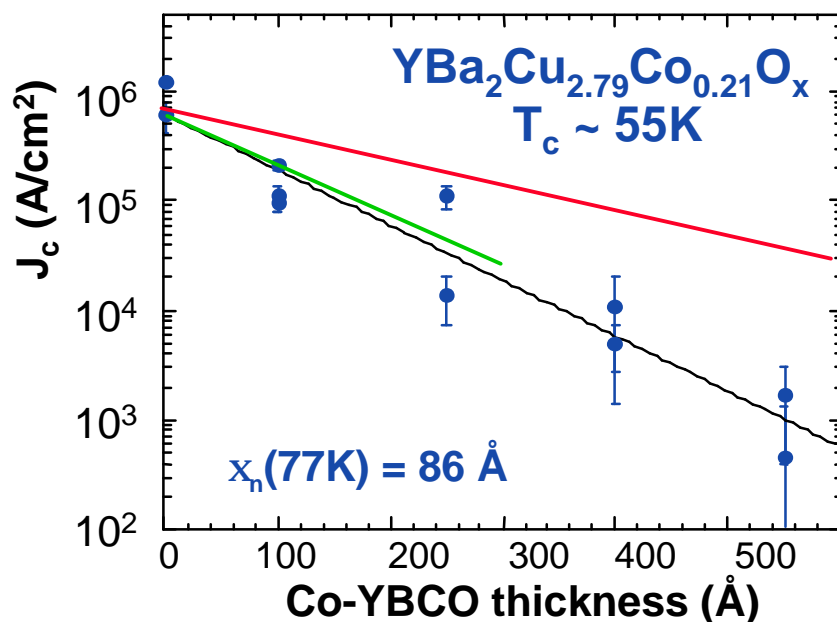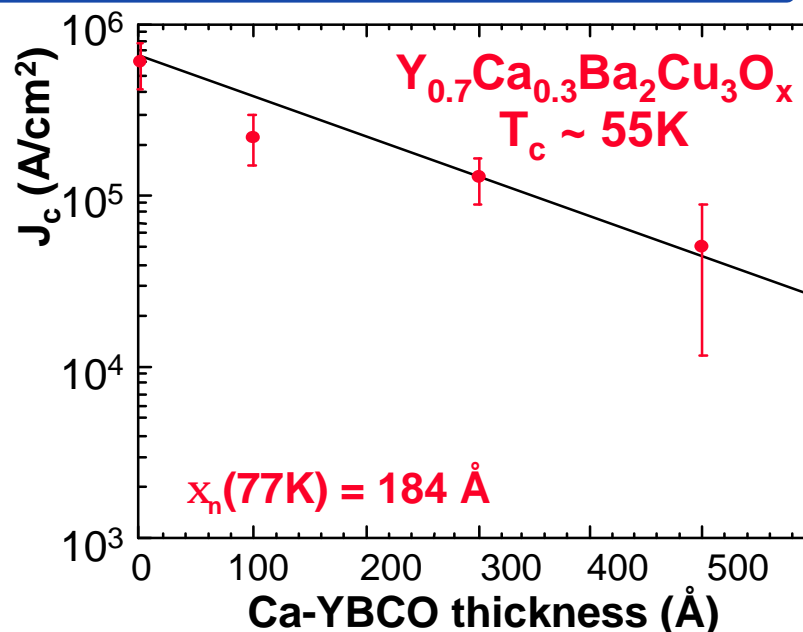$T_{cs} = 85\ K$
$T_{cn} = 45\ K$

$I_c\ (\mu A)$

T (K)

T (K)

$Y(x)$

L

S_1 N S_2

x_n x_s

- **Fits proximity effect model despite high resistance (~ 1 W)**
- **I_c vs N-layer thickness also fits model**

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Temperature Dependence of Critical Currents

- **19 junctions**
- **sputtered base electrode**
- **50 Å Co-YBCO**
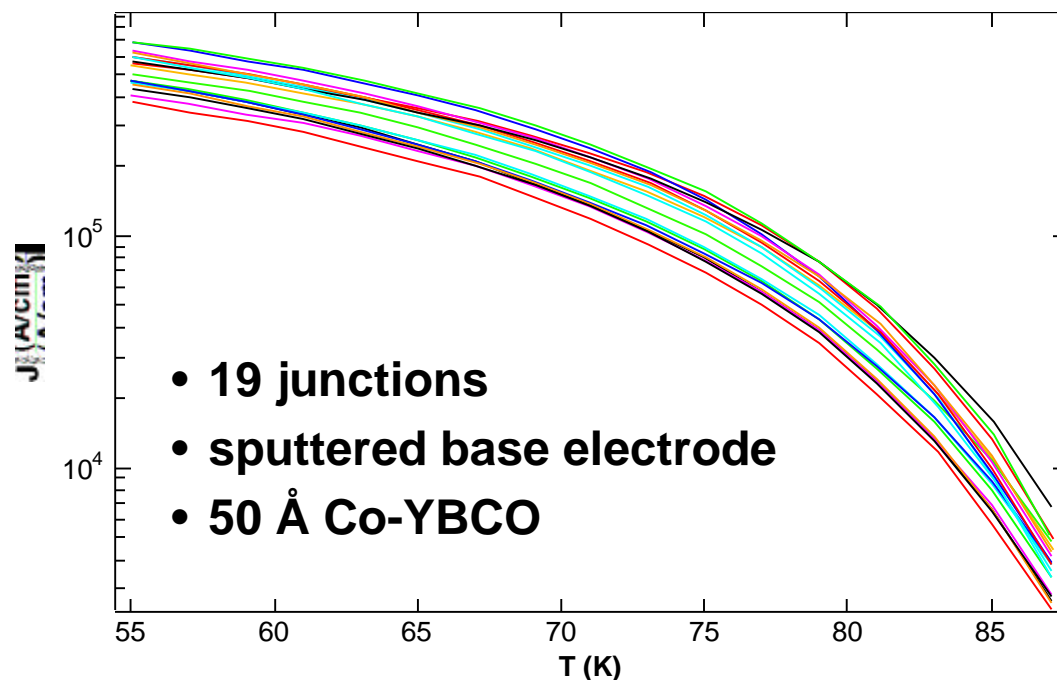
- **Curves tend to have same shape for all devices ⮕ suggests area variations predominant, rather than coupling across N-layer**

- **Requires interface resistance which does not significantly decrease inherent $I_c R_n$:**

  – **Patchy interface resistance to reduce the active area**

  – **or SINS (not SINIS) ⮕ e.g. insulator on base electrode edge**

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Exponential Behavior Observed for I_c vs. N-Layer Thickness

$Y_{0.75}Pr_{0.25}Ba_2Cu_3O_x$
$T_c \sim 65K$

$x_n(77K) = 96$ Å

J_c (A/cm^2)

Pr-YBCO thickness (Å)

$Y_{0.7}Ca_{0.3}Ba_2Cu_3O_x$
$T_c \sim 55K$

$x_n(77K) = 184$ Å

J_c (A/cm^2)

Ca-YBCO thickness (Å)

$YBa_2Cu_{2.79}Co_{0.21}O_x$
$T_c \sim 55K$

$x_n(77K) = 86$ Å

J_c (A/cm^2)

Co-YBCO thickness (Å)
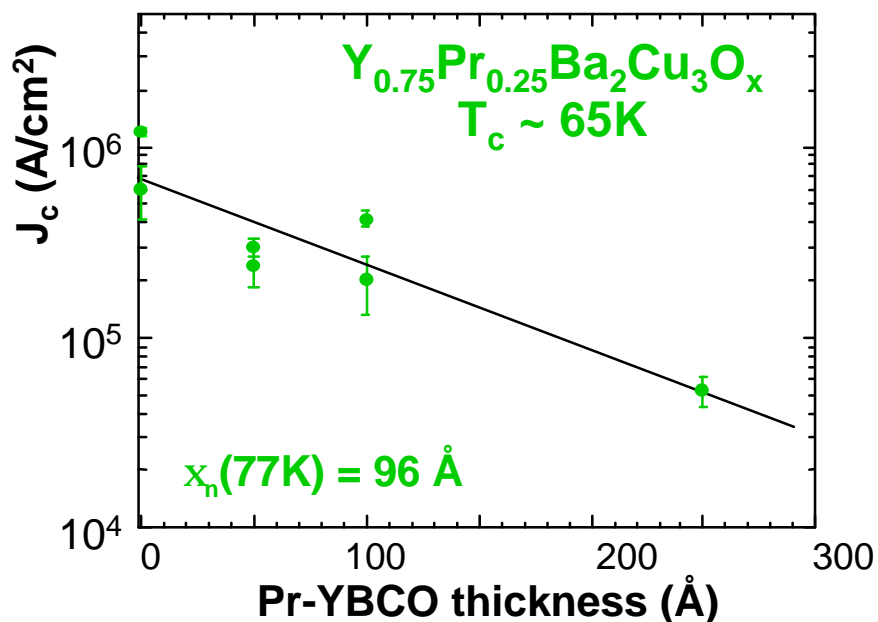
$$J_c \mu \ e^{-L/x_n(T)}$$

- Exponential behavior predicted by standard proximity-effect model

- Ca-YBCO has longest $x_n(77K)$ consistent with lowest $r(77K)$

- For all N-layer materials, x_n is 5x-10x larger than predicted by r

Continued Long-Term Progress in Junction Uniformity

- **Junction uniformity determines the level of circuit integration**
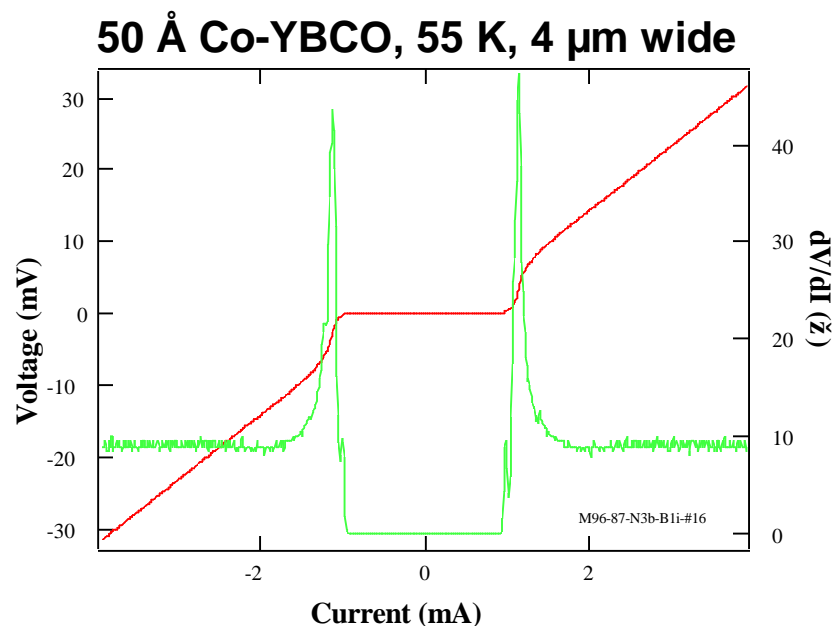- **Uniformity defined as inverse of standard deviation**
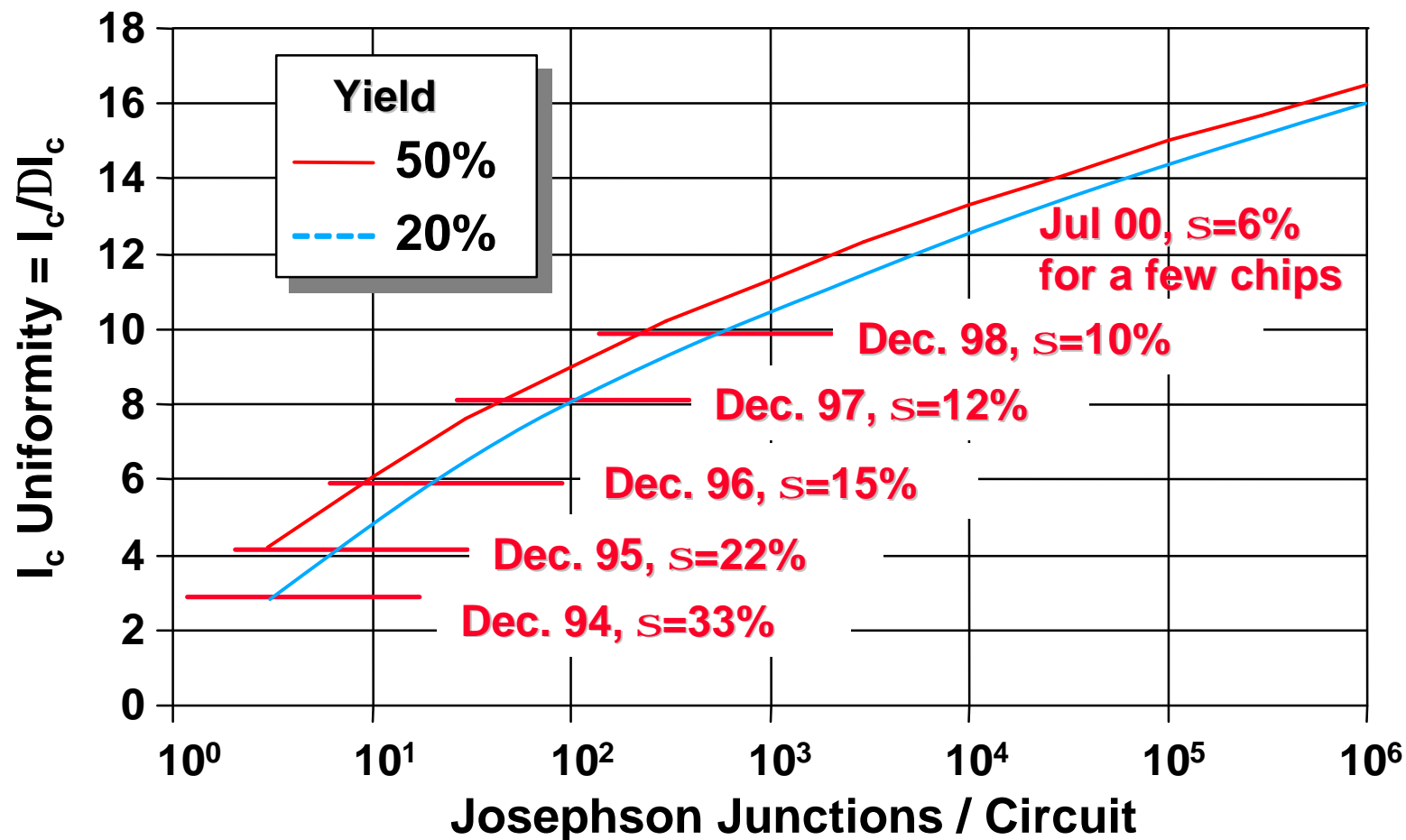
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I_c Uniformity in High R_n Series Arrays

50 Å Co-YBCO, 55 K, 10 μm wide
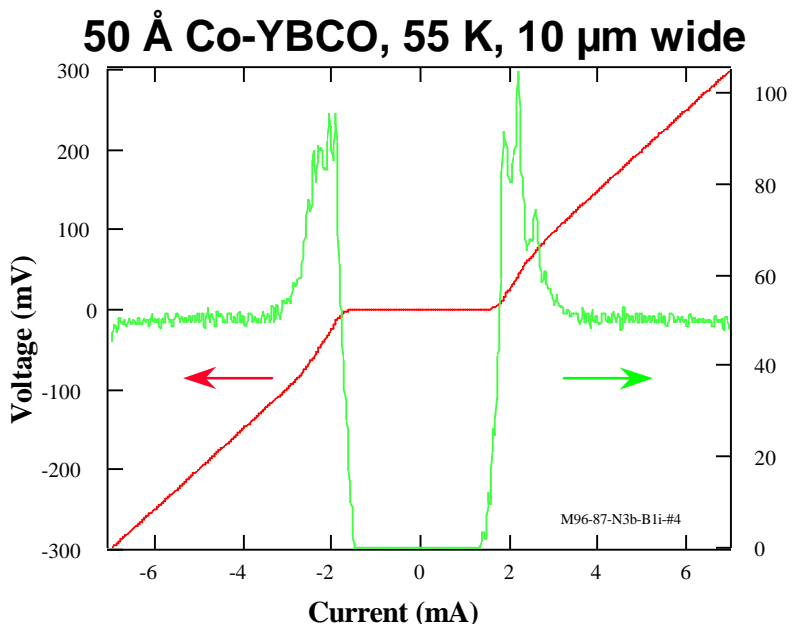
Ü 100 junction series array with $s_{Ic} \gg 11\%$

50 Å Co-YBCO, 55 K, 4 μm wide
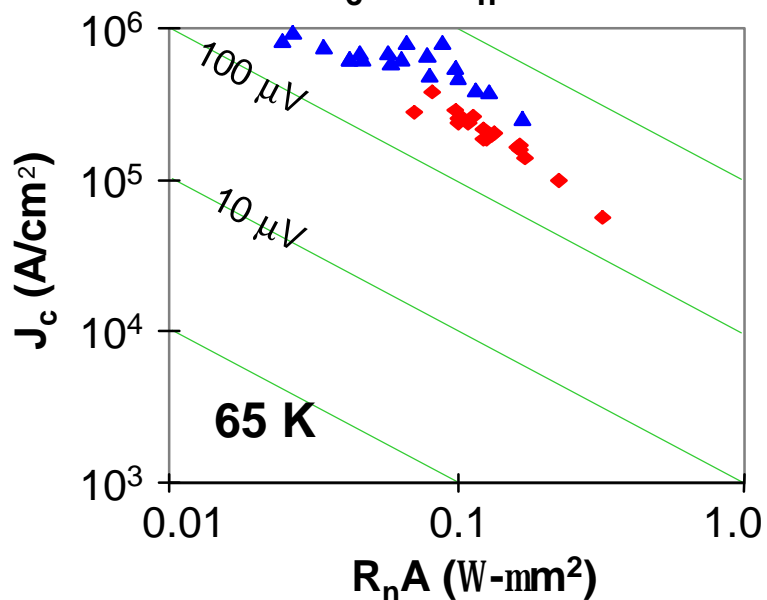

10 junction series array Þ with $s_{Ic} \gg 6\%$

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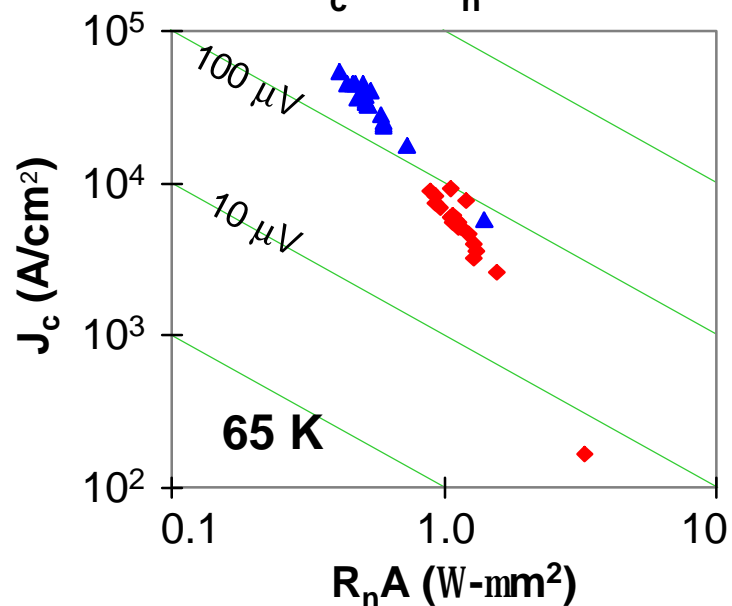
J_c vs R_nA Scaling for Junctions on a Single Chip

YBCO Base Electrode

J_c vs R_nA

La-YBCO Base Electrode

J_c vs R_nA

- **Constant I_cR_n indicates**
  1. Tunneling (SINS) with variations in barrier width or
  2. Reduced junction area with variations in effective area

- **Steeper slope in J_c vs R_nA indicates resonant tunneling or hopping conduction**
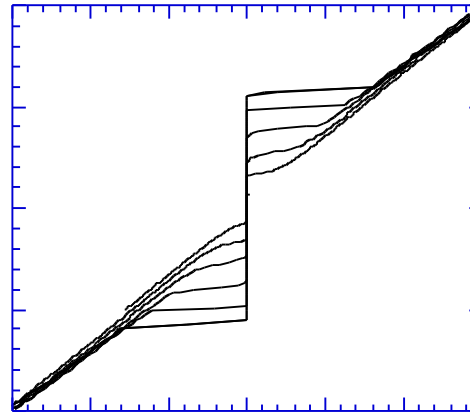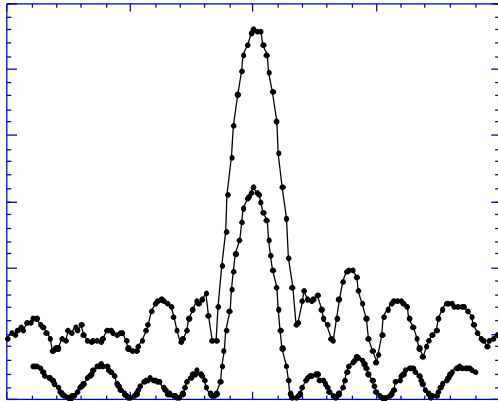 **-- What is the physical mechanism responsible for nonuniformity?**

◆ **Before plasma anneal**
▲ **After plasma anneal**

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Interface-engineered HTS junctions

Advantages

- Uses intrinsic properties of YBCO
- $R_n A$ tunable over 2 orders of magnitude
- Excellent uniformity: $s I_c < 8\%$
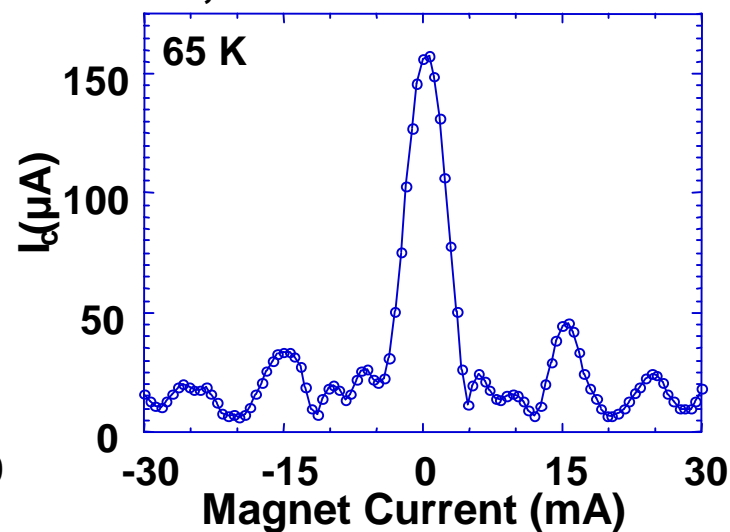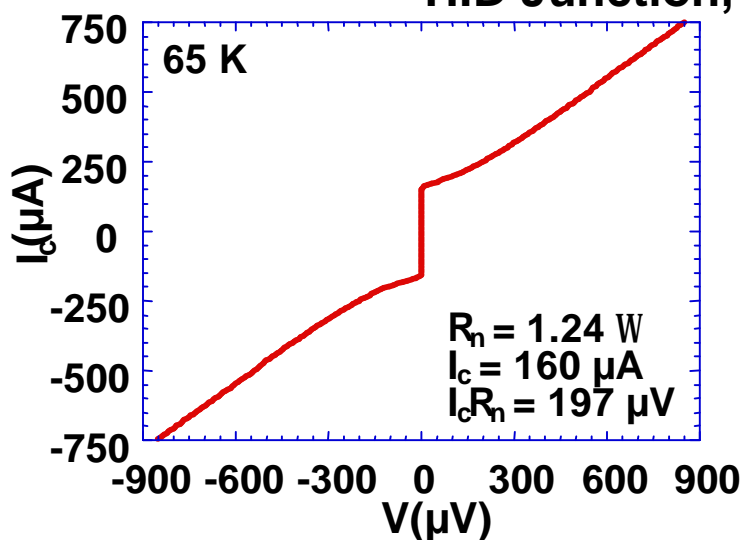- No deposited barrier

Disadvantages

- High-R_n devices not operable at high T
- Not yet good enough for multi-junction circuits

CONDUCTUS

HTS Junctions Formed by Edge Treatment Processes
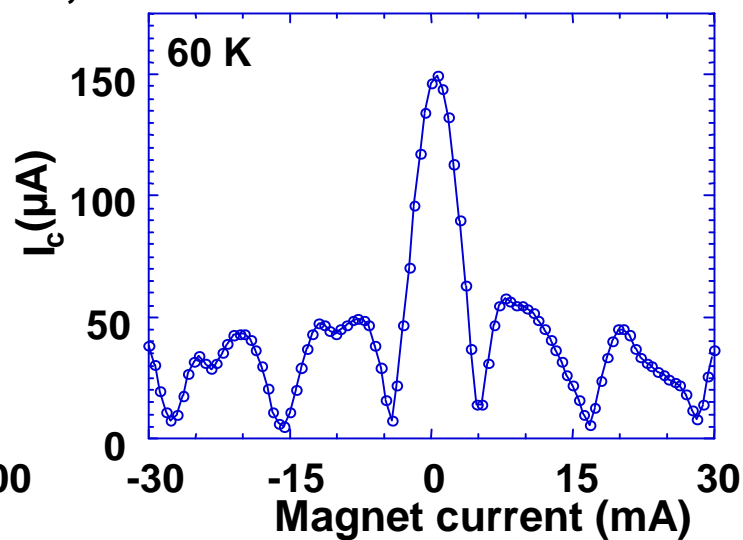
- Hot-Ion-Damage (HID) based on early JPL work and related to recent hot plasma process of Conductus ("IEJ") (also Japan, IBM)

- Relies on Ar or Xe ion beam to disorder base electrode surface

- Basic Hot-Ion-Damage Device ("HID") Process:
  - Standard ex-situ clean (O_2 plasma, Ar/O_2 mill, Br etch)
  - In-situ ion mill surface treatment at - 400ºC
    - 3-15 min. at 200V with 5 mA beam is typical
    - Ar YBCO mill rate is - 40-50Å in ten minutes
  - Vacuum anneal at - 400ºC   (following Conductus "IEJ" process)

- Special case of ion-mill time = 0 is Chemical Surface Treatment (CST)

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IV Characteristics for Edge-Treatment Junctions (no deposited N-layers)

HID Junction, 200 V Ar, 3 min

65 K

R_n = 1.24 **W**
I_c = 160 µA
I_cR_n = 197 µV

65 K

CST Junction, Br etch, 400ºC vacuum anneal

60 K

R_n = 1.9 **W**
I_c = 140 µA
I_cR_n = 266 µV

60 K
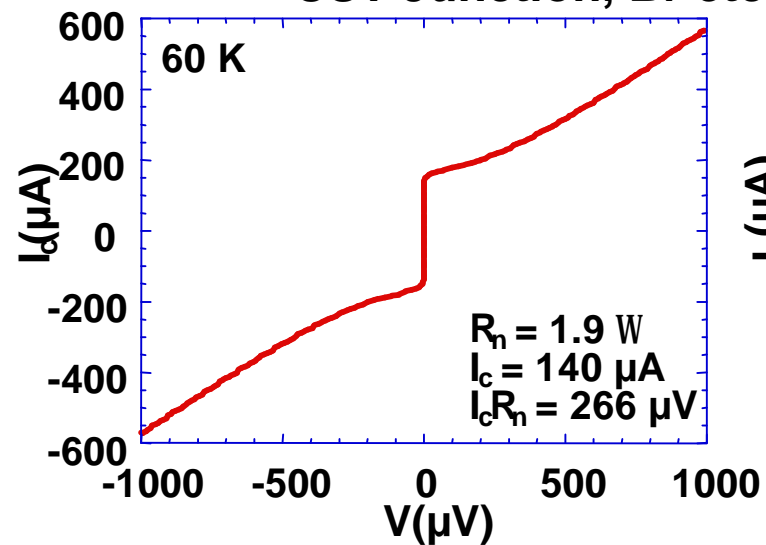
Integrated Resistor Process Developed for Modulator Circuits

- **Two resistor ranges required**
  - **0.5 -1.0 W/ square**
  - **few mW**
- **Ti / 0.2 mm Au bilayers on *in-situ* Au meet both requirements**
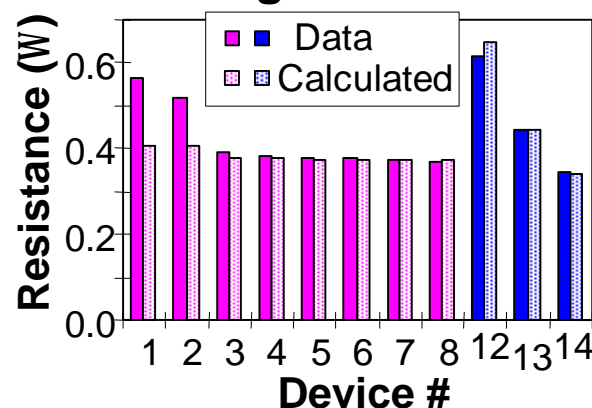- **YBCO / *in-situ*-Au contact resistance determines low-R values**
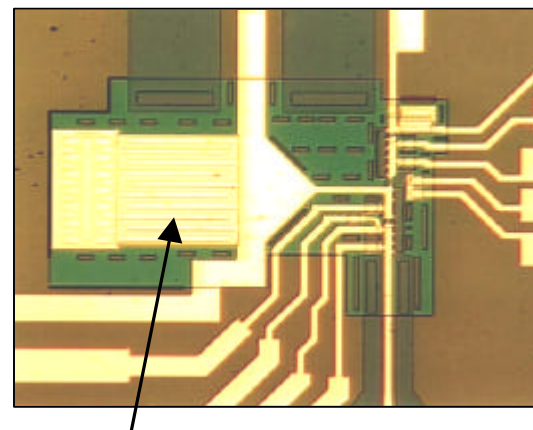
Interdigitated mW input resistor

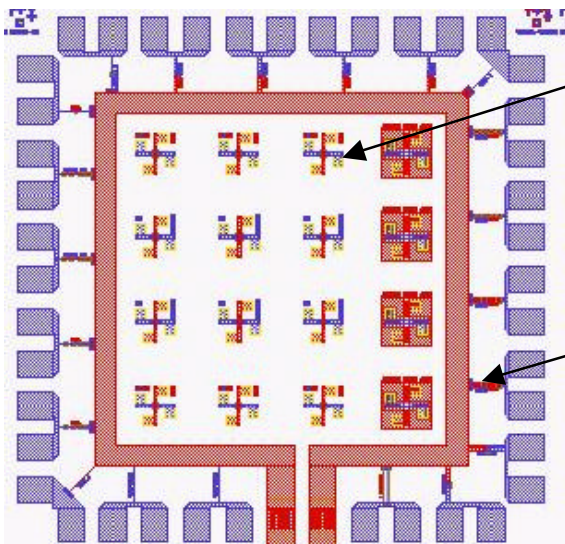### Resistance vs. length for interdigitated resistors

Au resistance

contact resistance

Resistance (mW) vs Finger separation (μm)
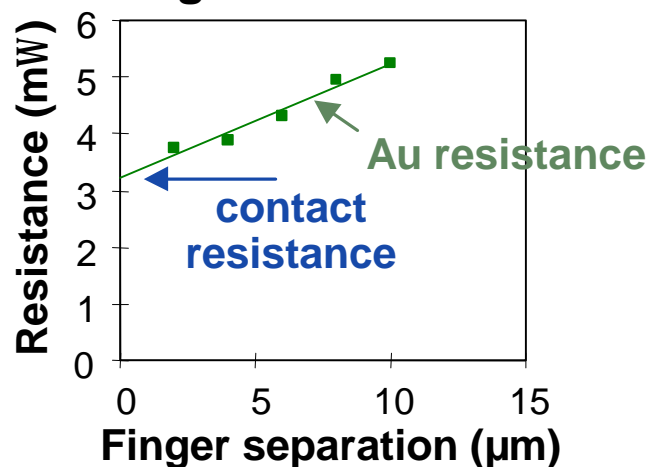
Resistance vs. contact area length and width

- Data
- Calculated

Resistance (W) vs Device #

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Via, Xover, & Step-Coverage Test Devices Designed, Fabricated, & Evaluated for HTS Circuits

44-Pin Test Sub-chip (1 of 4 per chip)

Probe Station Meas:
10^4 **mm**^{2} **capacitors and isolation meas.**

Individual Test Bridges:
single & series
vias & Xovers

YBCO-1 J_c Bridge under Insulator

YBCO-2 J_c Bridge on Insulator

YBCO-2 across Insulator Trench

YBCO-2 / YBCO-1 Crossover

c-axis Via

a-axis Via

Oxygen-Diffusion Structure

20 mm

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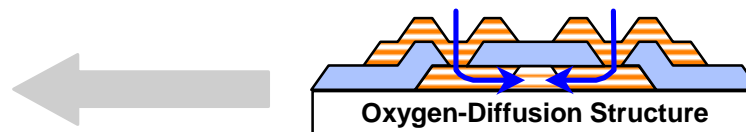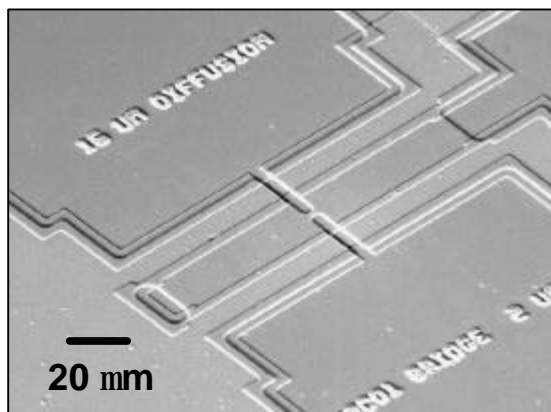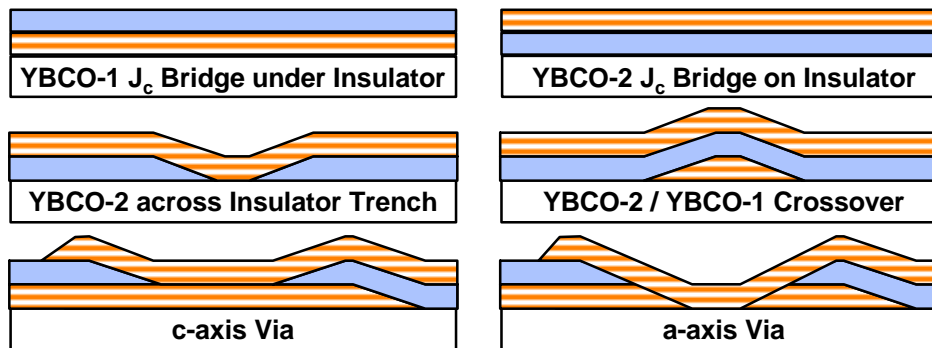
Accomplishments: Processes Developed for Crossovers, Vias, and Oxygen Diffusion

Crossover J_c

J_c (A/cm^2)

- ▲ No steps
- ◆ ...over 20 STO steps
- ■ ...over STO & YBCO steps
- ● SEGB SQUID
- ▲ SNS JJ

Temperature (K)

Oxygen Diffusion and T_c in YBCO / SAT / YBCO

T_c (K)

Plasma Oxidation

1 atm O$_2$ Anneal

T96-39-N1
4 µm devices

Diffusion Distance, d (µm)
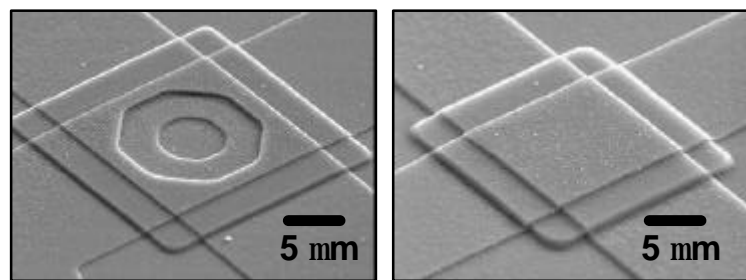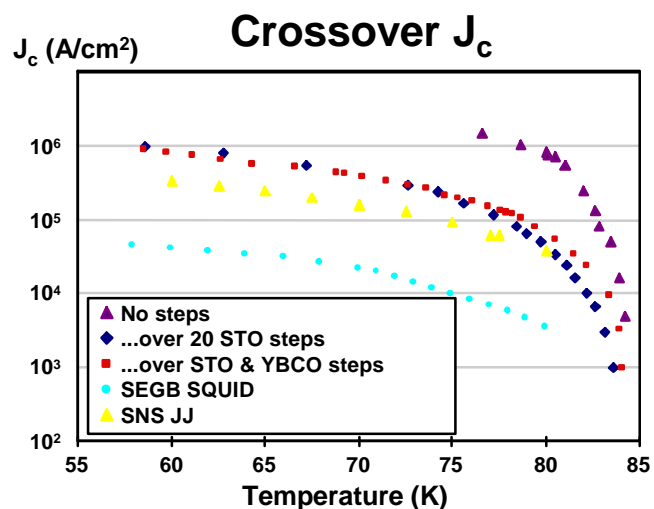
- **Critical currents for passive devices, J_c >> junction critical currents**
- **Low-e, low-tan d SAN and SAT insulators replacements for STO**
- **a-b plane oxygen diffusion measurements determined coef**
  - **7×10^{-9} cm^2/s, in agreement with literature values for single crystals --- impractical times**
  - **invention of "oxygen vias"**

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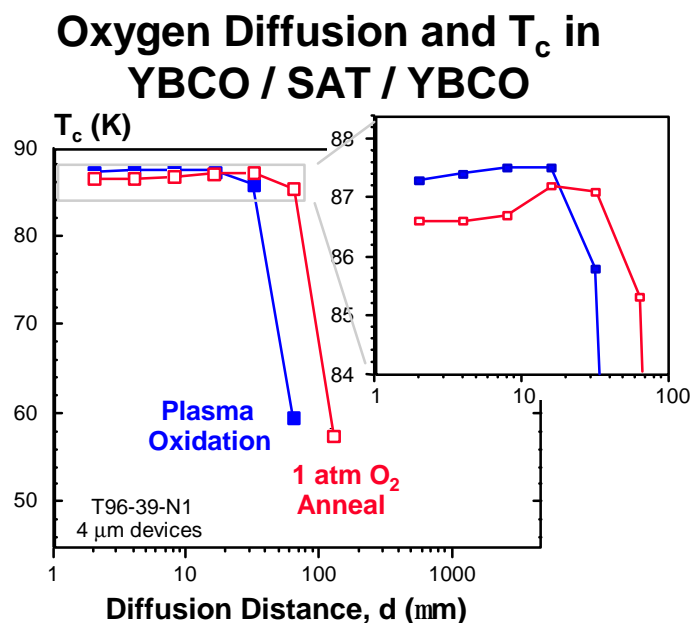
Innovations Used for Modulator Circuits: Mask Layout with "Oxygen Vias"

- **With improvements in YBCO film smoothness and insulator integrity, even 4-day oxidation anneals at 450ºC cannot restore x   6-90-6.95 in YBCO$_x$ ground planes**

- **Cooling in oxygen plasma provided solution before changeover from SrTiO$_3$ to SAN and SAT insulators**

- **Measurements of a-b plane oxygen diffusion rates in films agreed with single crystals and determine "oxygen via" spacing and oxidation times**

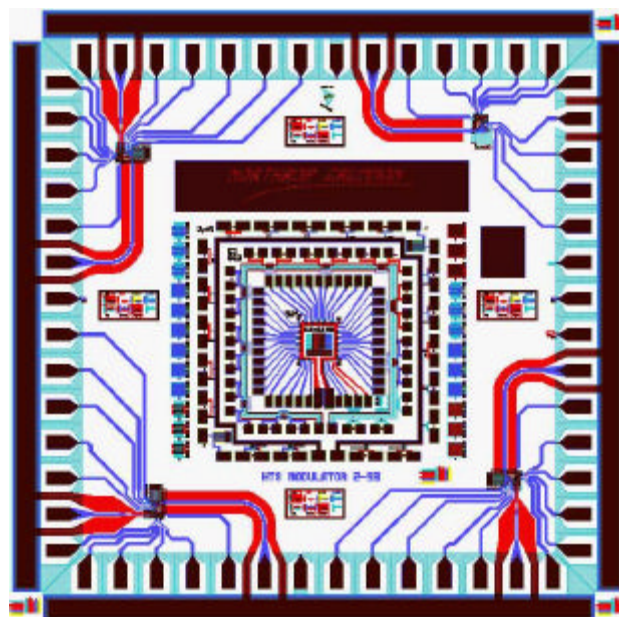**Holes in blanket groundplane insulator**

10 mm
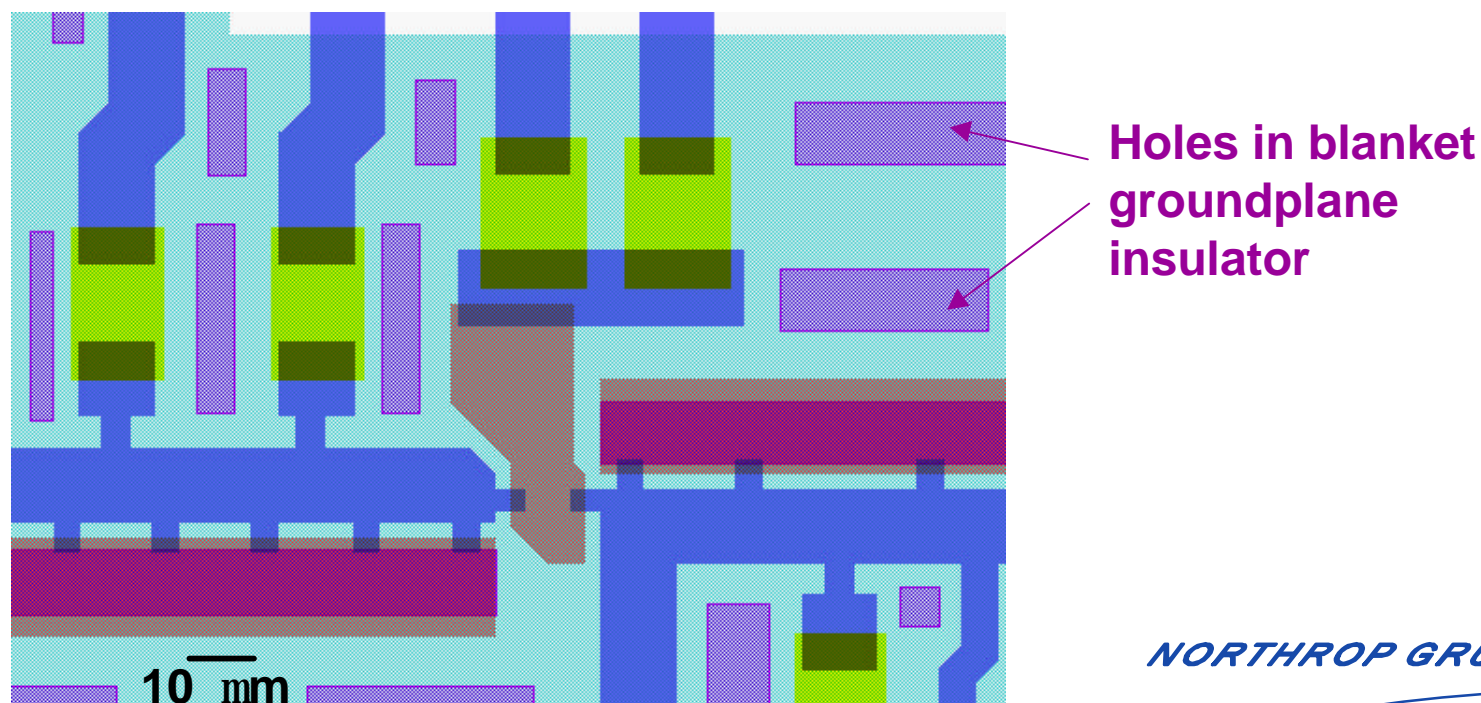
NORTHROP GRUMMAN
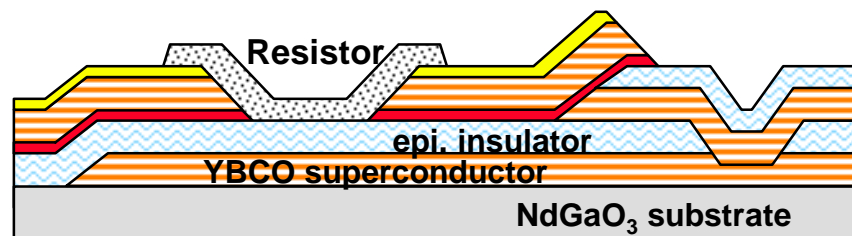
Approach: Same Chip Dies Couple Circuit Development to Process Development

- **Multiple circuit copies to experiment with component values and layout parameters**
- **Multiple PCM subchips for process development**

Circuit Cross Section

Resistor

epi. insulator
YBCO superconductor
NdGaO$_3$ substrate

Circuits

PCM Vias/xovers/bridges

PCM SQUIDs

PCM Junctions

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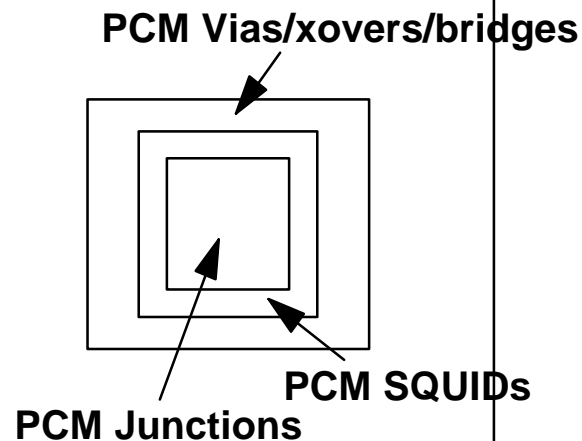
HTS SFQ T-Flip-Flops Operate at 65K

Satyr T-FF

20 µV/div
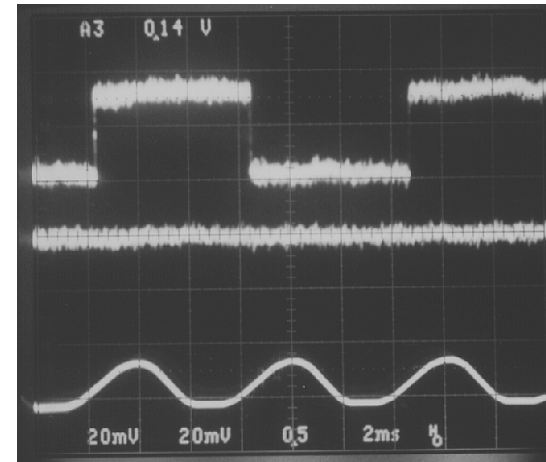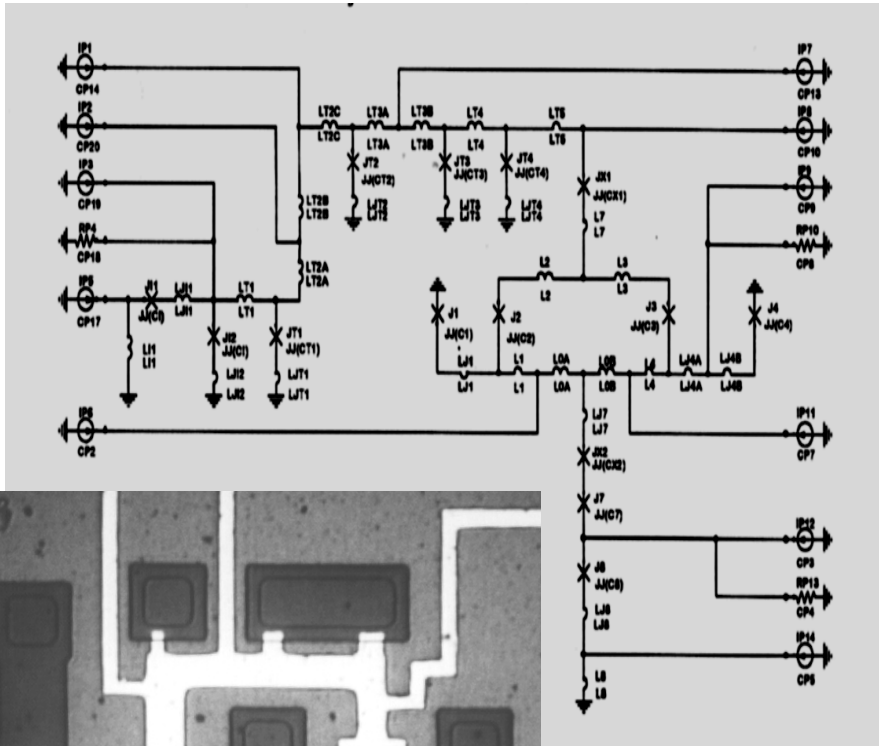
Readout

FF Voltage
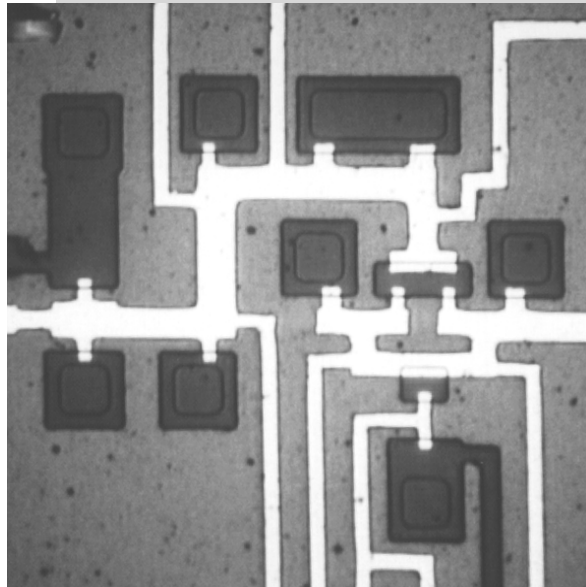
SFQ Gen Input

T-Flip-Flop
- **Satyr**
- **Triton**

Triton T-FF

20 µV/div
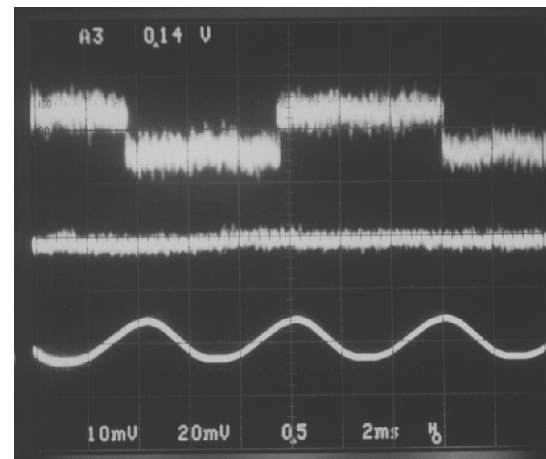
Readout

FF Voltage

SFQ Gen Input

(Dale Durand, TRW)

4-Bit Counting A/D Converter for Low-Power Operation

- **39 junction circuit fabricated with extendible process**
- **All four T flip-flops can store flux & be read out**
- **First bit toggles with input current**

SFQ/DC   SFQ/DC

DC/SFQ → JTL → T → JTL → T → JTL

T → SFQ/DC

JTL

T → SFQ/DC

JTL

10 mm

55 K

Input current (0.5 mA/div)

Bit 1 output (50 µV/div)

NORTHROP GRUMMAN
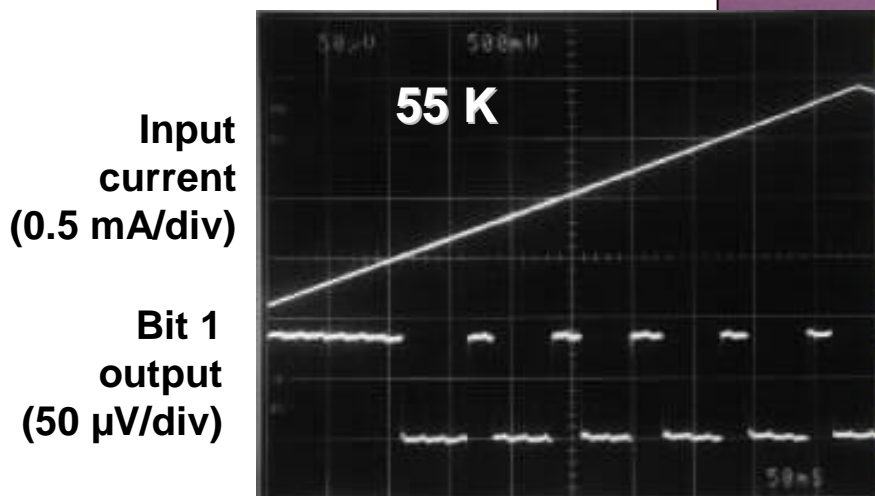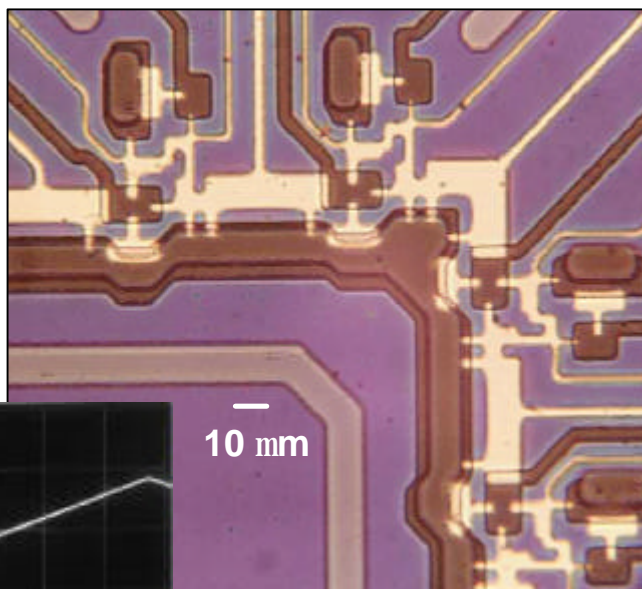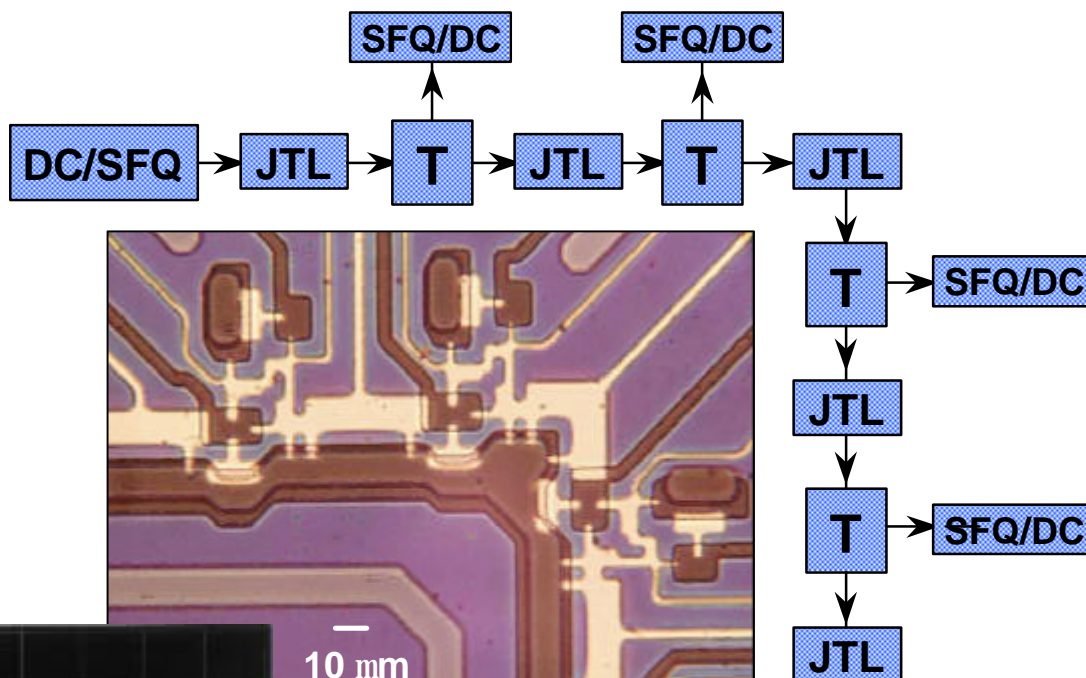
Voltage Divider Utilizing HTS Ramp-edge Junctions with a Ground Plane
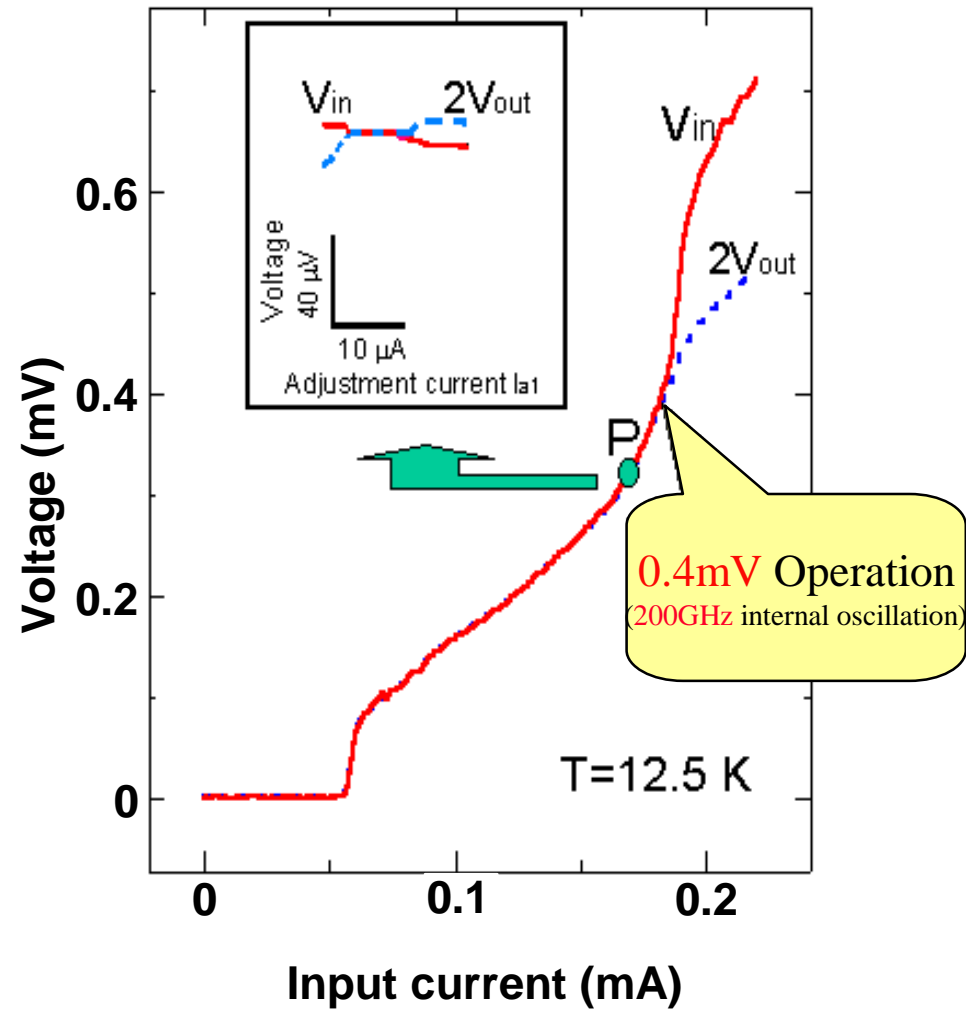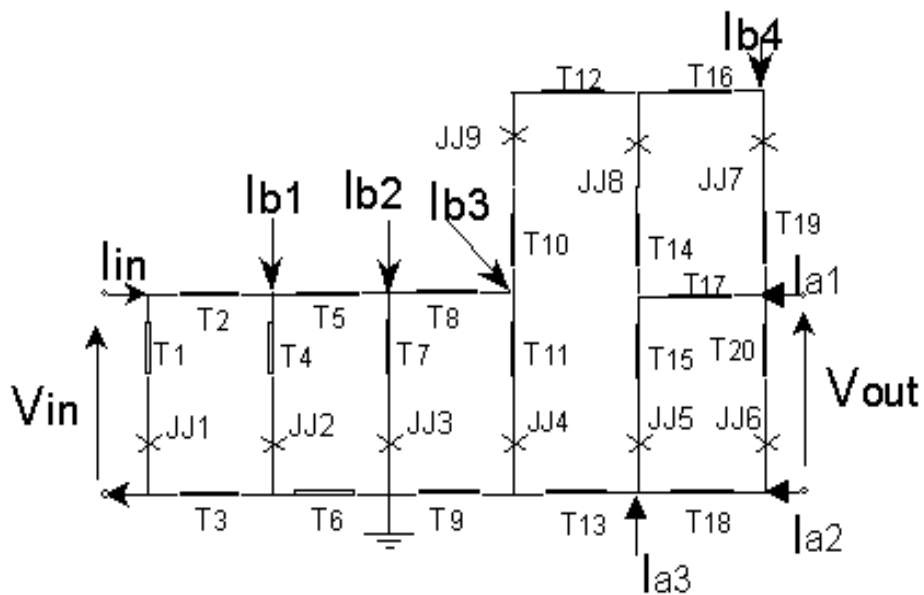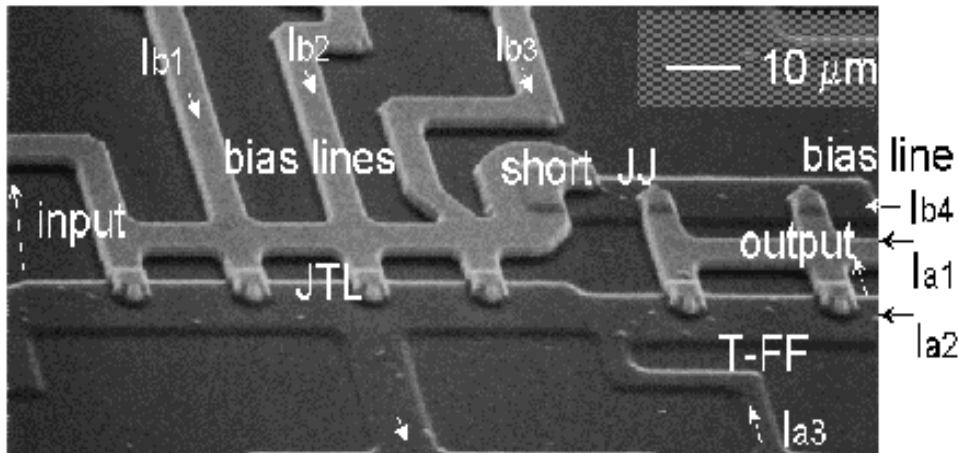
TOSHIBA

Summary of Worldwide Progress in HTS Junctions & Circuits
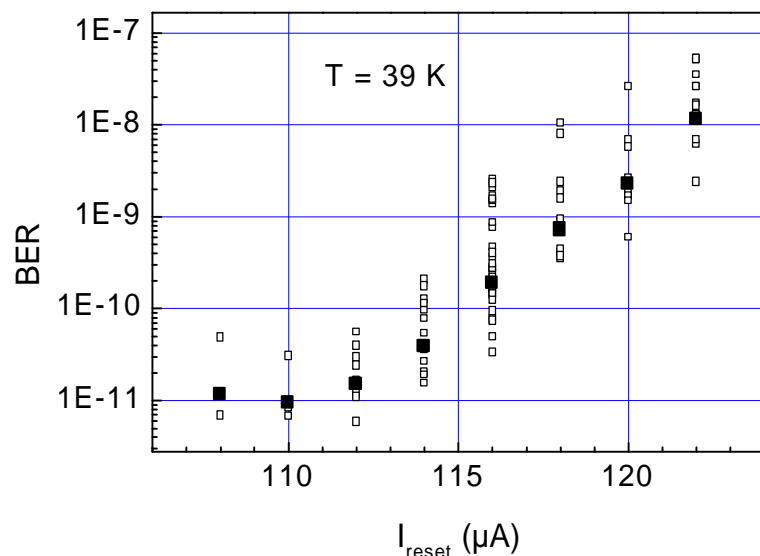
Measurement of BER < 10^{-11} in HTS at 39K (KFA Jülich)

"Modified interface" 100 junction series array with I_c s = 8% (NEC)

4.2K
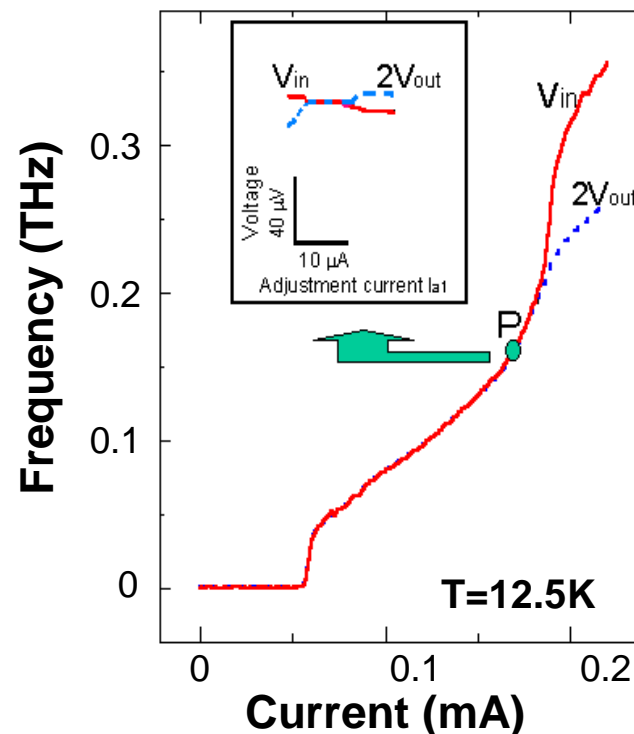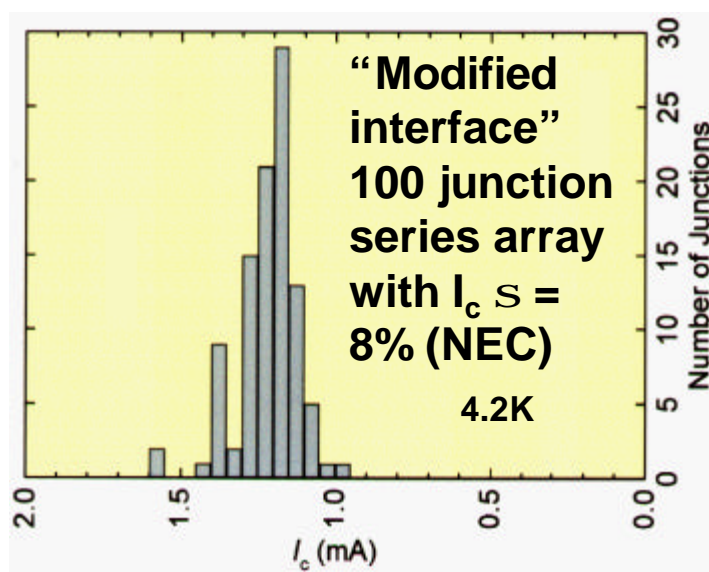
Toggle flip-flop @ 200GHz with extendible process (Toshiba)

HTS Sampler (NEC)

$I_{trigger}, I_{r2}$ $I_{signal}, I_{feedback}, I_{r1}$
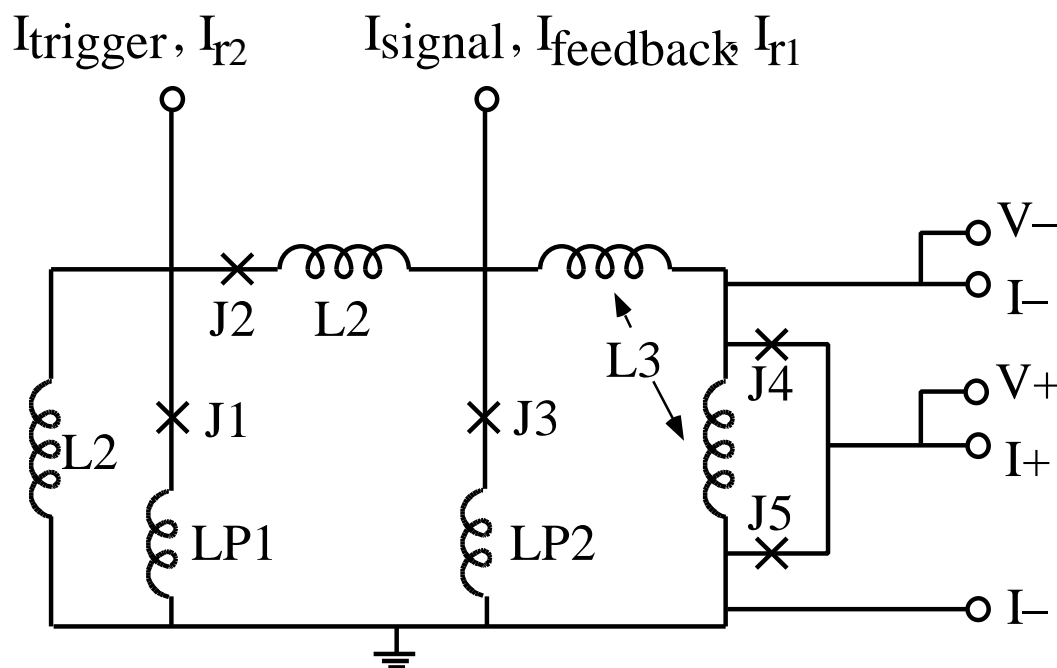
- **High $I_c R_n$ => good time resolution**

- **60K Þ 0.5 mV Þ 3.5 ps 2 mV Þ < 1ps**

- **Thermally-limited sensitivity $\delta I \sim 0.15$ μA @ 60 K**

- **50 W Þ $\delta V \sim 7.5$ μV**

- **GaAs sampler ~ 100 mV @ comparable time res.**

J2 L2 V− I− L3 J4 V+ I+ J1 J3 L2 J5 LP1 LP2 I−

M. Hidaka & J.S. Tsai, IEEE Trans. Appl. Supercond. Vol. 5., No. 2, June 1995
M. Hidaka, H. Terai, T. Satoh, & S. Tahara, ISEC '97, Paper D54

HTS Technology Enables CRYORADAR™ to Find Targets in Clutter

Cryoelectronic Radar Subsystems Provide:

Pure Transmit Signal

- 100x increase in microwave resonator Q
- 50x increase in dynamic range
- 50x reduction in size

Low Noise / High Dynamic Range Reception

- 10x increase in speed
- 10x reduction in power of logic circuits
- ~20 dB improvement in target detectability in clutter
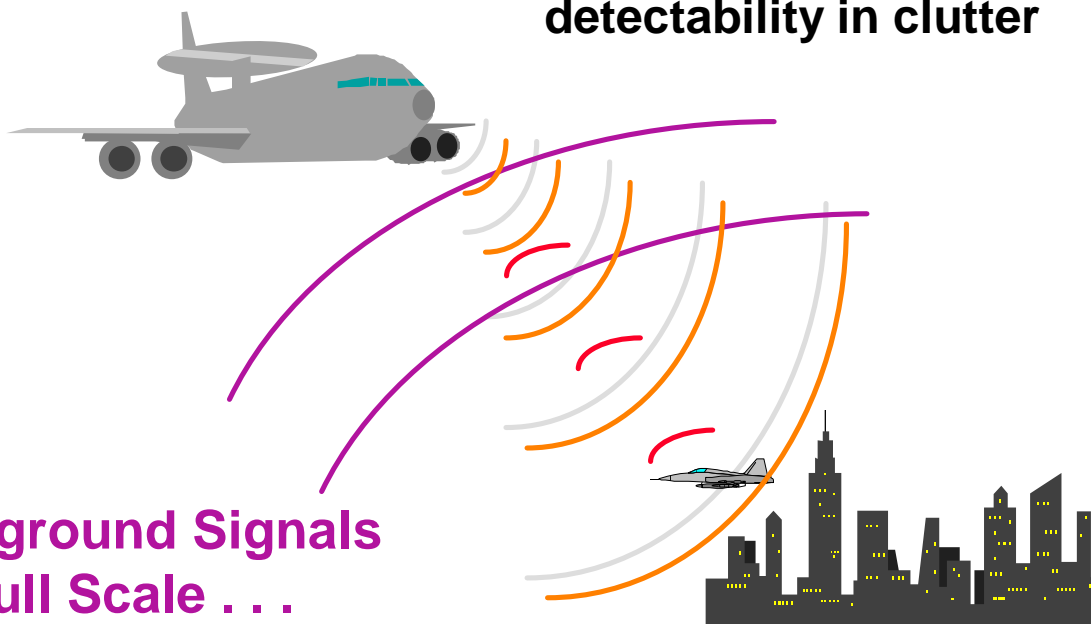
**Large Background Signals Establish Full Scale . . .
but Small Signals Can Be Important**

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Josephson-Based Circuits Are Needed to Exploit Low-Phase-Noise STALOs

Cryo STALO

- **Significant Improvement in Radar Sensitivity (Limited by state-of-the-art ADC)**
- **Demonstrated in Navy Radar Testbed**
- **Integrated cryocooler**

Transmit ...

STALO   **Waveform Generator**

Josephson AC Voltage Standard → **Multiple transmit frequencies**
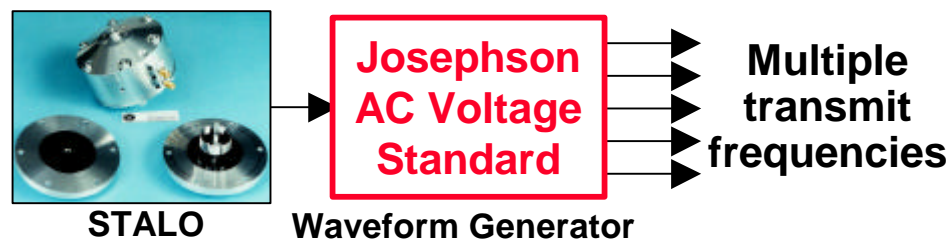
- **Avoid jamming**
- **Track scintillating targets**
- **Minimum junction count, ~ 100-300**

... Receive

Josephson High Dynamic Range ADC

- **Quantized flux provides linearity in the feedback mechanism of ADCs with S-Δ architecture**
- **Junction count, ~ 350-1000**

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Digital (Mixed-Signal) Subsystems for CRYORADAR™

Low-noise DACs and High-dynamic-range ADCs

HTS DACs are based on the same physics as the US standard volt and new NIST initiative for ac voltage standards

- **Josephson junctions convert frequency of pulses to a voltage level**
- **5 GHz   Junction parameters of $I_c R_n \gg 10$ mV**
  $I_c \gg 1$ mA
  $R_n \gg 0.01$ W

HTS ADCs designed in Σ-Δ architecture

- **Quantization of magnetic flux used for precise feedback**
- **Switching speed needed for oversampling**
- **500 GHz   Junction parameters of $I_c R_n \gg 1$ mV**
  $I_c \gg 0.5$ mA
  $R_n \gg 2$ W

- **In Japan, Σ-Δ ADCs for "software radio"**

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ADCs and DACs:
The Right Niche for HTS Josephson Technology

- **Workshop on Superconductive Electronics: Devices, Circuits, & Systems, 9/97, CMOS working group:**
  - *"Deeply scaled CMOS not likely to support high-dynamic-range ANALOG functions ..."*

- **ADCs and DACs are principally analog circuits**
  - **Precision tracking/generation of analog signals**
  - **Bit error rate requirements modest ($< 10^{-6}$)**
  - **Junction count << e.g. processors**

- **Use properties unique to superconductivity**
  - **Flux quantization**
  - **ac Josephson effect**

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Junction Non-Uniformity Motivates Applications with Low Junction Counts

Spread in Critical Currents, s_{Ic}

Northrop Grumman HTS Digital Demos

Sigma for 20% Yield

Sigma for 50% Yield

Low-Power Counting ADC

High Dynamic Range ADC

Spread Spectrum Modem

Network Switch

Number of Junctions in Circuit
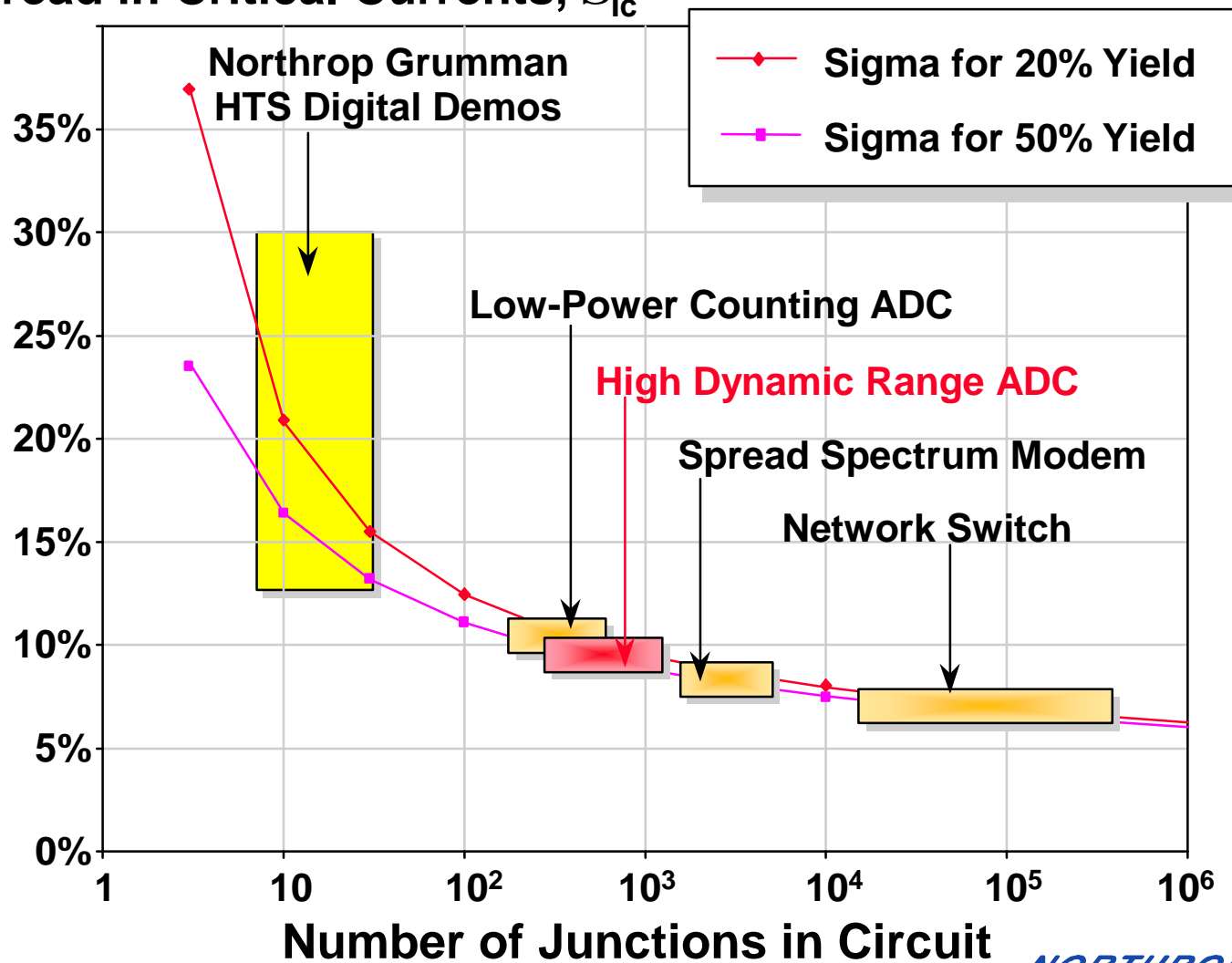
NORTHROP GRUMMAN

Northrop Grumman's Approach

- **Sigma-Delta architectures for linearity**
  - **quantization errors remembered and compensated**
  - **oversampling and feedback to balance the incoming signal**
  - **standard in the audio recording industry**
- **Parallel materials technologies:**
  - **LTS for fastest progress in circuit development and availability for shipboard deployment**
  - **HTS fabrication development for airborne deployment**
- **Teaming with NIST on WFG**
  - **closely related to JJ-based ac voltage standard**
- **Teaming with universities on HTS fabrication development**

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Quantized Feedback is the Essential Advantage of an SFQ Design for S- D

- **Sigma-Delta ADCs use oversampling and feedback for high dynamic range**

- **Semiconductor ADCs balance input with electrons on capacitors. Not repeatable.**

- **Superconductor ADCs balance input with flux quanta. Repeatable. Accurate.**
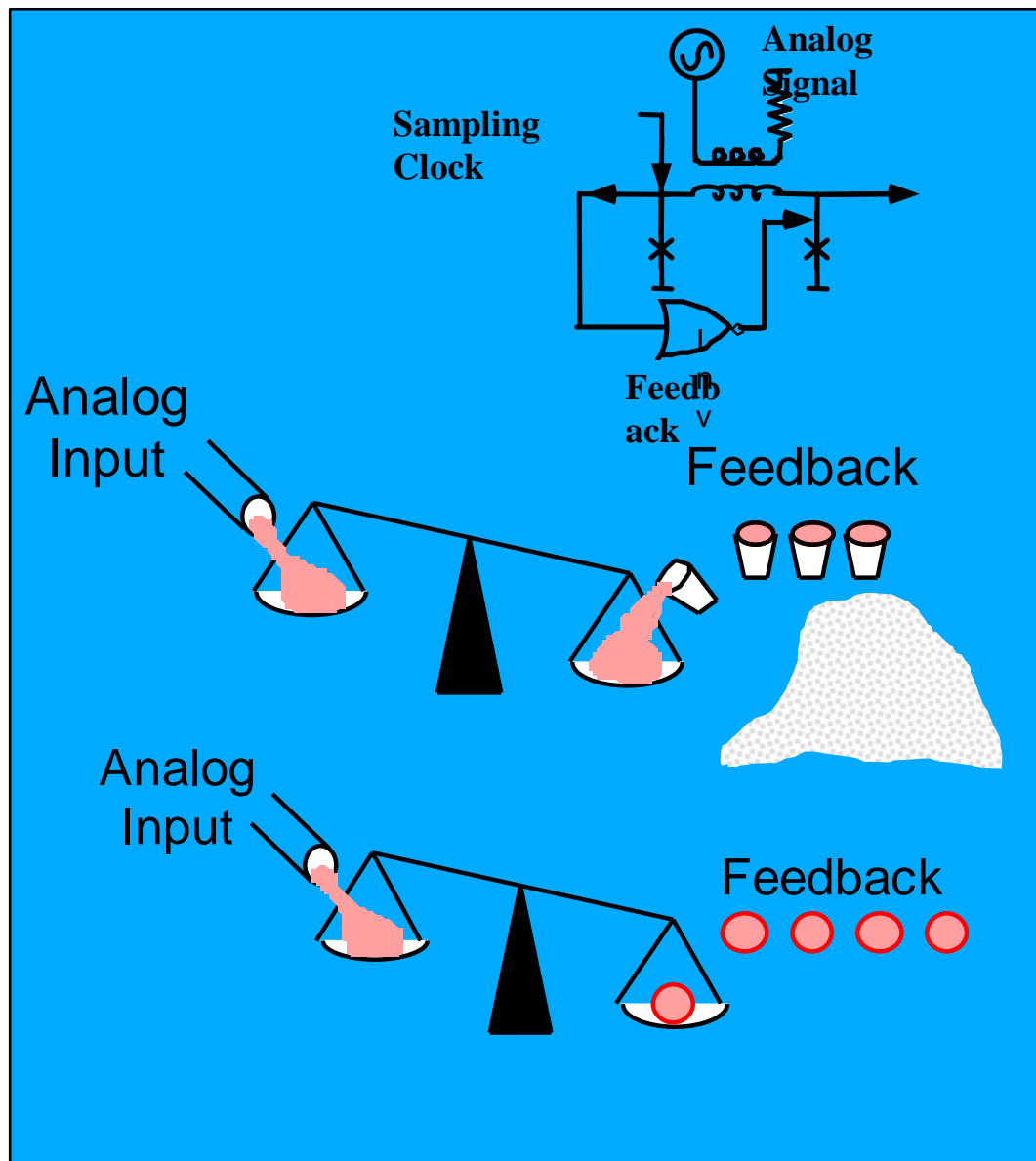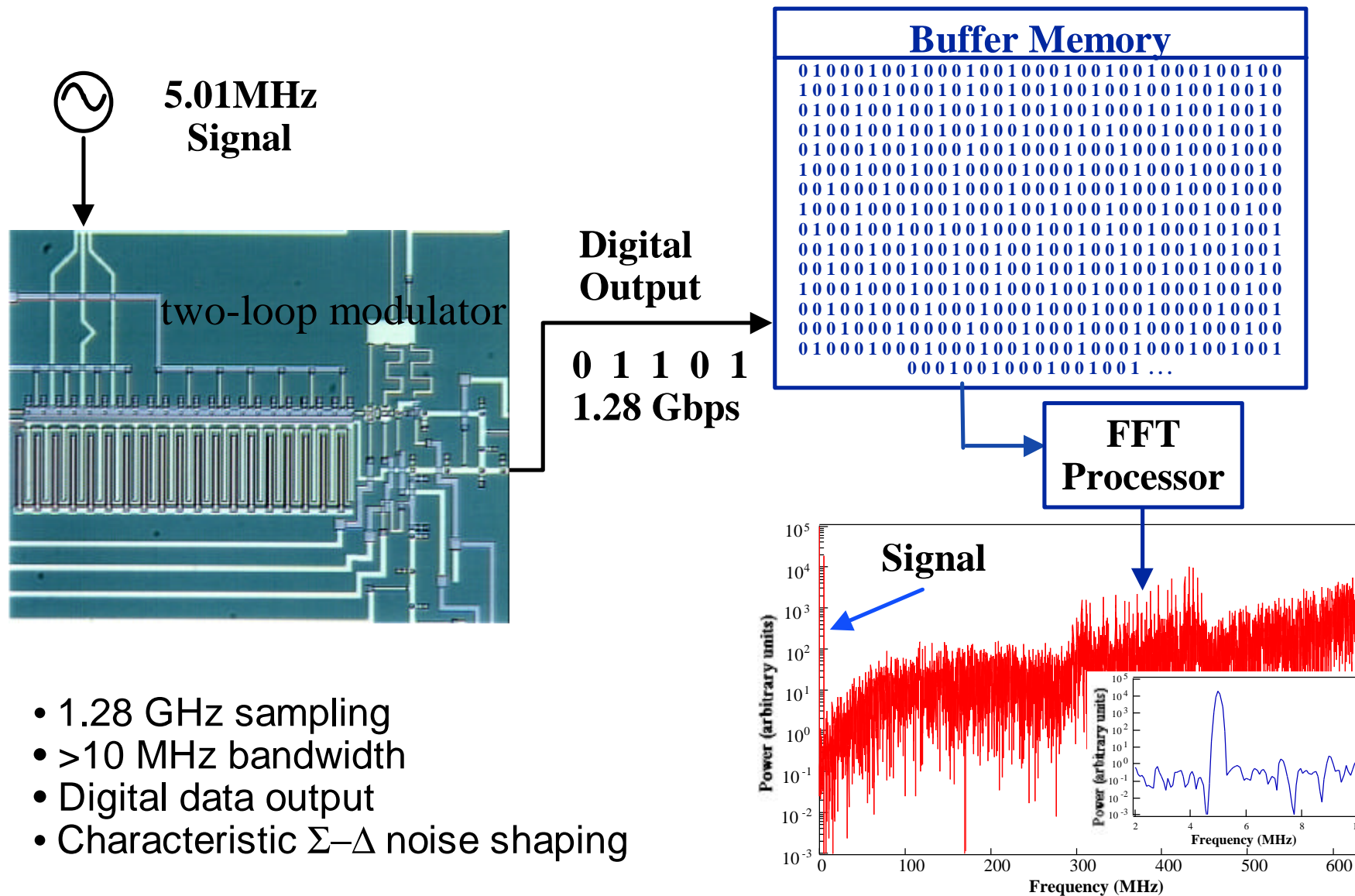
Hybrid ADCs Will Leapfrog the Rate of Progress for Purely Semiconductor ADCs
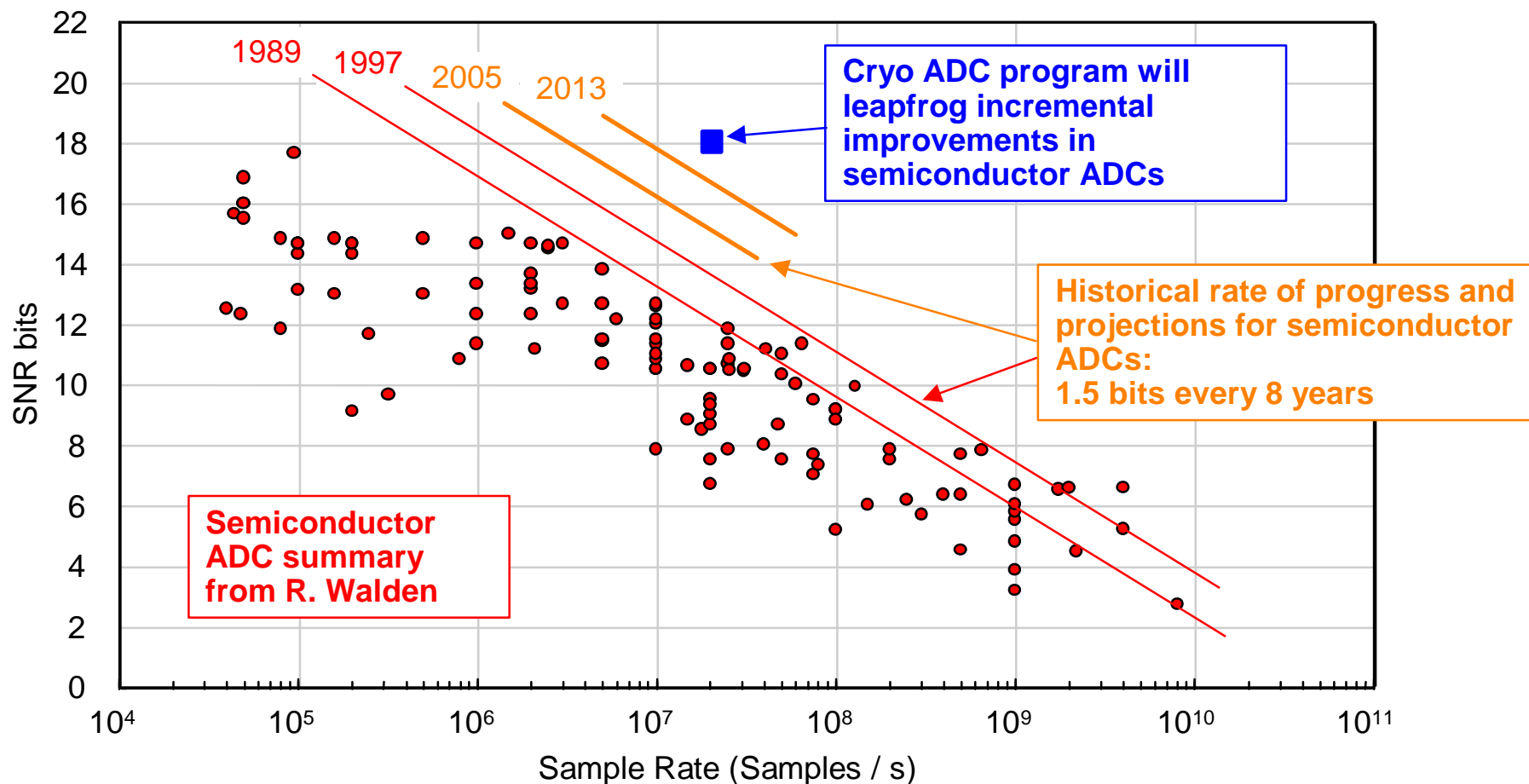
- **Hypres' Approach: All-superconducting, LTS-only architecture, 10^4 junctions**
- **Northrop Grumman Approach: Super/Semi hybrid, HTS-compatible design, ~350 junctions**

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Proof of Principle Demonstrated in JJ ADC Noise Shaping

5.01MHz Signal

two-loop modulator

Digital Output

0 1 1 0 1
1.28 Gbps

Buffer Memory

FFT Processor

Signal

- 1.28 GHz sampling
- >10 MHz bandwidth
- Digital data output
- Characteristic $\Sigma-\Delta$ noise shaping

Linearity Demonstrated for HTS Single-Loop Σ-Δ Modulator

HTS circuit demonstrated

- **27 GHz clock**
- **SFDR > 75 dB**

- **Third order intermod products -58 dBc**
- **First HTS demonstration of rf signal conversion**

20 mm

T = 35K

10 dB

5 MHz signal

10 MHz har-monic is below noise floor

200 Hz

— Output at 5 MHz
— Output at 10 MHz
— Output at 10 MHz with no signal

27 GHz sampling

5 MHz input signal

Clock

Signal Input

Sampler

Output

NORTHROP GRUMMAN
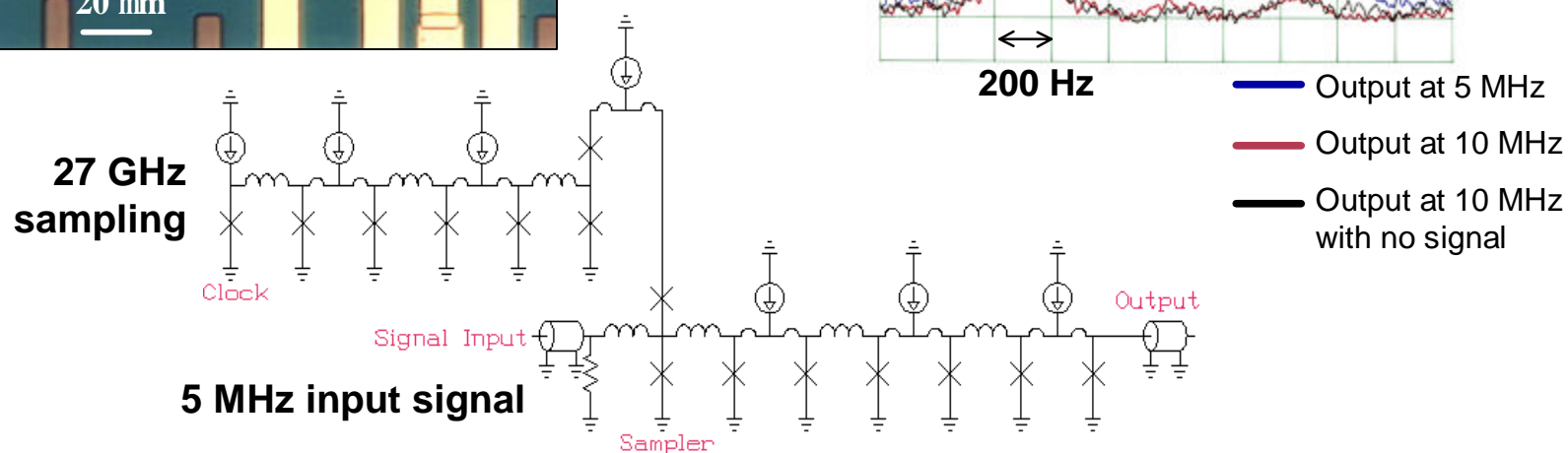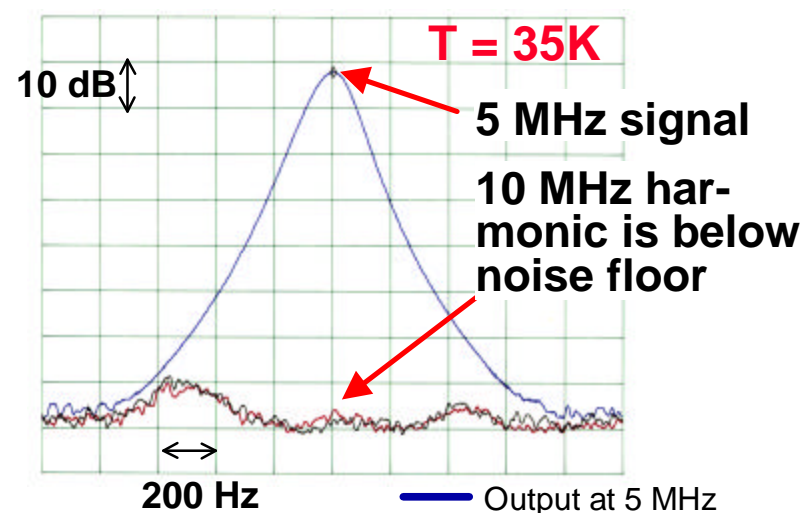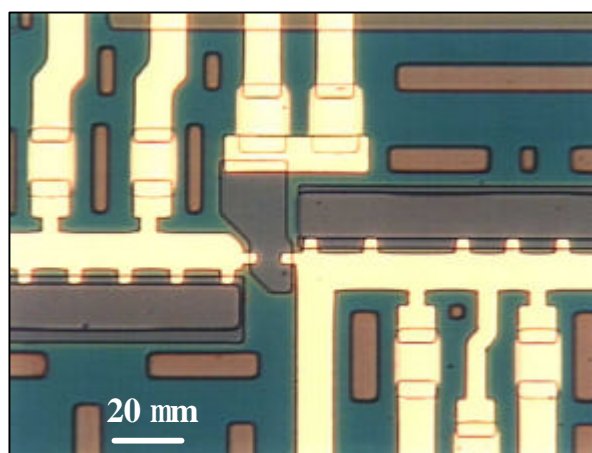
Conclusions

- **Digital HTS electronics are based on circuit speed, low power dissipation, and exploitation of the unique property of flux quantization**

- **Non-uniformity of HTS junction critical currents limits the junction count in circuits to ~100**

- **Most important near-term "digital" HTS subsystems are mixed-signal circuits (ADCs and DACs) requiring just 100s of junctions**

  - **Two ranges of Josephson junction parameters required**

  - **LTS circuits used to develop and validate circuit concepts**

  - **HTS junction integration with groundplanes and passive devices demonstrated in small-scale circuits**

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